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7 May 1982

USSR Report

CYBERNETICS, COMPUTERS AND AUTOMATION TECHNOLOGY

(FOUO 7/82)

EXCERPTS FROM

'COMPUTERS AND COMPUTER NETWORKS'

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COMPUTERS AND COMPUTER NETWORKS

Moscow EVM I VYCHISLITEL'NYYE SETI in Russian 1980 (signed to press 20 May 80) pp 2-3, 283-303, 326-327

[Excerpts from book "Computers and Computer Networks", by Vasiliy Nikolayevich Kriushin, Inna Nikolayevna Buravtseva, Nina Mikhaylovna Pushkina and Nina Grigor'yevna Chernyak, Izdatel'stvo "Statistika", 18,000 copies, 328 pages]

[Excerpts] Annotation. The functional principles of computers and systems are outlined. The material is based on third-generation computers.

Basic attention is devoted to logic organization of computers and systems, the characteristic features of encoding economic data, the structure of peripheral equipment, the characteristics of individual devices and their operating capabilities. The principles of designing collective-use computer networks, the equipment included in the networks and user interaction with the computer are considered.

The material in the textbook corresponds to the curriculum of the course "The Configuration of Computers and Computer Networks" for students at higher educational institutions studying specialty No 1738. The book will be of interest to students and specialists working in the field of computer applications in automated control systems and at computer centers.

Introduction

At the present time there are roughly 3,000 computer centers in the country [3]. More than 3,000 automated control centers were in use at the beginning of 1977 [2]. In 1978 alone more than 400 automated control systems for accounting, planning and management were set up [32]. More than 300,000 specialists in the country are working on development and operation of automated control systems [33].

Contents

Chapter 11. Communications Systems

11.3. Information Transmission Equipment

The enormous importance of communications equipment was pointed out by V. I. Lenin, who wrote in 1918 that "socialism without the mails, telegraph and machinery is an empty phrase."*

Selecting the means of communication depends on a large number of factors: the number of users, the speed and reliability of transmission, the length of the communications channels and so on. Telegraphic communications equipment is most efficient in those cases which require high reliability of transmission, telephone communication equipment is preferable for higher speed and facsimile communication equipment is best for transmitting drawings and figures.

*"Polnoye sobraniye sochineniy" [Complete Works], Vol 27, p 278.

The basic equipment used in telegraphy comprises various types of telegraph operation. The contemporary models use the modified international telegraph code MTK-2 recommended for use by the International Telegraph and Telephone Consultative Committee. This code is a uniform, five-element code in which zero is transmitted by an absence of current and one is transmitted by the presence of current. For this reason all electrical components are divided accordingly into currentless and current components.

Each combination transmitted by telegraph channel in MTK-2 code has a length of $5t_o$, where t_o is the length of a single signal. However, when telegraph equipment operates in the start-stop mode, two additional service components are introduced. The first one, the start, being without current, is transmitted before the code combination and also has a length of t_o. The second component, the stop, which completes transmission of the code combination and has the current position "1," is longer--1.5-2.0 t_o. Thus, the total length of one code combination transmitted by telegraph channels in MTK-2 code is 7.5 t_o.

In addition to the general characteristics described above, various other indicators are used to define telegraph operations:

correcting capability, which characterizes the quality of work of the telegraph apparatus and is determined by the magnitude of maximum marginal distortion with which it is still possible to record an error-free signal. This capability may be theoretical, effective (that is, measured under real operating conditions) and nominal (which is the lowest for a group of similar devices);

theoretical probability, equal to the maximum number of words which can be transmitted and received by the telegraph apparatus in an hour;

technical productivity, which takes into account the time of transmitting useful information and service information;

operating productivity, which reflects the design characteristics of the equipment, operator qualifications and so on.

All telegraph equipment is basically similar in design and has the following primary functional parts:

the transmitter, which enters and converts the information to be transmitted. It comprises a keyboard, a coding device with five steel bars, each of which may occupy one of two fixed positions corresponding to "1," and "0," by which the coding device carries out the coding, the transmitting distributor, whose primary purpose is to convert parallel code combinations formed by the bars into a sequence of electrical signals. The rotational frequency of the distributors, which is a fixed value in all telegraphs, determines the length of a single signal t_o;

the receiver, whose functions are to receive, convert and print the information received from communications channels on papertape. The receiver consists of a distributor which performs the inverse conversions relative to the transmission, the decoder with five decoding bars and a printer;

a drive mechanism;

auxiliary assemblies and devices, including mechanisms to feed the paper and inking tapes, the register switch mechanism, a self-locking device and so on.

Telegraph lines use the domestically produced ST-35, ST-2M, STA-2M, RTA-6, STA-M67, RTA-7 and other telegraph equipment plus the East German T-51 and T-63 units.

The STA-2M telegraph, which is a modification of the ST-35, uses MTK-2 code. It has a speed of 50 bauds and a maximum operating range of 550 kilometers. The letter "A" in the STA-2M telegraph means "automated" because transmitter and reperforator attachments are connected to it, which permits it to be used for transmitting a prepunched tape and for receiving information from the channels on both papertape and punch tape.

The availability of these attachments leads to full use of communications channels and the capability of preparing punched tapes in advance makes it possible to improve the quality. Moreover, the use of punched tapes permits automation of the message relay operations at central telegraph stations and makes it possible to use punch tapes as information carriers for computers.

The STA-M67 telegraph differs only slightly from the STA-2M.

The page-printing start-stop telegraphs were a further development of telegraph technology. The RTA-6 page-printing telegraph with transmitter and reperforator operates at a speed of 50 and 75 bauds, has a roll of paper 215 millimeters wide and can receive three copies of text simultaneously.

The RTA-7 page-printing telegraph, unlike the electromechanical devices considered above, is classified as an electromechanical telegraph in which certain mechanical assemblies such as the distributor, coder, decoder and a few others are replaced by electronic devices. The RTA-7 operates at speeds of 75 and 100 bauds and has three registers, automated attachments, a noise suppression filter, a radio receiver and a number of other auxiliary units.

Telegraph communication can be organized using either general-purpose communications included in the system of USSR Ministry of Communications and serving various institutions and the public through a network of communications departments or by means of user telegraphy, which serves those institutions that have telegraph equipment connected to the user telegraph station.

One of the varieties of user telegraph equipment is the international Telex telegraph, designed for transmitting messages to other countries.

Facsimile communications apparatus is used to transmit fixed images (documents, photographs, drawings, tables, textual material and so on) through communications channels. According to the definitions of the International Telegraph and Telephone Consultative Committee, the terms "phototelegraph" and "phototelegraphic apparatus" should refer only to the equipment used to transmit and

receive half-tone images. The more general term is "facsimile apparatus,"* related to devices that transmit both half-tone and facsimile originals.

There is a fairly broad range of facsimile communications equipment including the following devices:

FTA-PM, Aragvi and Shtrikh, which are used only for receiving and transmitting facsimile images measuring 220 X 150 millimeters (220 X 300 millimeters in the FTA-PM), they have transmission times of 12.5, 6 and 2.1 minutes, respectively, and the image is printed on ordinary paper;

Ladoga, designed to transmit hydrometeorological charts of unlimited length and up to 480 millimeters wide. A sheet measuring 480 X 690 millimeters requires 22 minutes for transmission;

Neva is used for working with both half-tone and facsimile originals. It requires 6 minutes to transmit an original measuring 220 X 300 millimeters;

Gazeta-1 and Gazeta-2 are used to transmit newspapers; for this reason they are larger than the original (420 X 610 millimeters), can receive copies on photographic film and have a more rigid requirement for misalignment of images--not more than 1 millimeter for each 100 millimeters of the page. The devices can transmit one newspaper page in 50 and 2.3 minutes, respectively.

All facsimile devices consist of transmitting and receiving parts. The transmitting part includes: a scanning device for breaking the image of the original down into elements, a light-optical system by means of which a light beam is moved across the surface of the original secured to the surface or a revolving drum (as a function of planar or cylindrical scanning), a photoelectric converter that converts the light reflector from the original into electricial pulses whose value depends on the image brightness, a video signal converter, phase and synchronization devices and so on.

The basic devices of the receiving part of the facsimile apparatus are the video signal converter, the recording and scanning devices and the phase and synchronization units. They convert electrical pulses fed from the communications channel into a luminous flux which is then projected onto the surface of photographic paper (this method is called the closed method because the image becomes visible only after the photographic paper is properly processed) or onto electrochemical, electrothermal and other types of paper (this method is called open because the copy appears immediately upon receipt).

Among the traditional means of communication are varieties of telephone equipment, including the TA-60, TA-65 and TA-72 (Soviet Union), TsB 621/65 and TsB 631/65 (Poland), V = 63 St (East Germany), TA-66a (Czechoslovakia) and others, the ATS-47, ATS-54 and ATSK automatic telephone exchanges and so on.

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*A facsimile is an exact reproduction at the receiving station of the image being transmitted.

Among the various means of communication, the most attention is devoted to building and using data transmission equipment (APD). This usually includes an error protection device (UPZ), designed to enter verification symbols to protect the data being transmitted against errors, a memory unit whose capacity must be sufficient to store at least one code combination, a control device which provide for interaction among all assemblies of the data transmission equipment, input-output devices and a signal conversion unit (UPS).

The signal conversion unit is used because the data to be processed by computer are written in binary form and represented by square-wave pulses. No additional operations are ordinarily required to transmit them by telegraph channels. But the data must be appropriately converted to transmit them by telephone channels, which is done by using a sc-called carrier frequency selected in the middle of the bandpass and the data are entered in it. This process, called modulation, greatly increases transmission speed. Modulation can be frequency (the frequency of the carrier oscillation is subject to variation), amplitude or phase.

Modulation is accomplished in special devices called modems which generate the needed sine curve and modify it according to data received. Demodulation of the carrier frequency is also carried out in modems.

Some of the data conversion units such as the Akkord-50, the Akkord-1200 and the Minsk-1500 (Figure 11.4) operate in a semiduplex mode that provides data transmission by telegraph channels at speeds of 50 and 100 bauds. Transmission reliability is $3 \cdot 10^{-7}$. Information is entered from papertape by an FF-1500 photoreader (Czechoslovakia) and retrieved to papertape by a PL-150 tape punch that is connected to the Akkord-50 by a remote integration, perforation and reading unit. Information is entered and also retrieved by page-printing telegraph. Connections are made using the call device included in the Akkord-50 set. Cyclic coding and resolving feedback are used to ensure good-quality transmission.

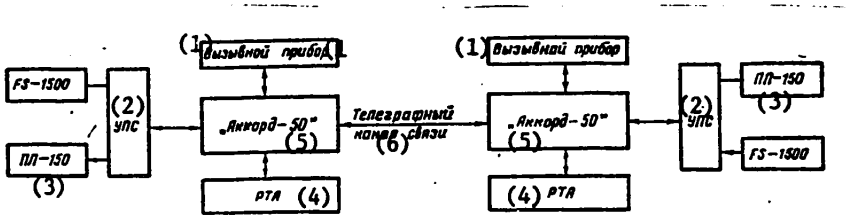

Figure 11.4. Block Diagram of Data Transmission Using the Akkord-50 Data Transmission Equipment

Key:
1. Call device
2. Signal conversion unit
3. PL-50 tape punch
4. Page-printing telegraph
5. Akkord-50
6. Telegraph channel

The Akkord-1200 data transmission equipment is used for working with telephone communications channels and functions both in the semiduplex (switched channels) and duplex (segregated channels) modes at speeds of 600 and 1,200 bauds. High reliability of data transmission (no worse than 10^{-6}) is achieved by using cyclic codes with the polynomial $x^{16} + x^{12} + x^5 + 1$ and resolving feedback. The Akkord-1200 operates in the following modes: "telephone," which is designed for service communications, "data transmission," which only transmits data, "data reception," which only receives data and "internal," which is used to check the working condition of the equipment.

The Akkord-1200 set of equipment includes a PL-150 tape punch, an FS-1500 photoreader, a calling and ringing device and an Akkord-1200 PP transceiver. If the user station does nothing but transmit data, it will have an Akkord-1200 PD transmitter operating in three modes: telephone, data transmission and internal, instead of the Akkord-1200 PP. The transmitter has a coding device that forms the check combination of the cyclic code, a data input control unit that converts parallel code into series code, writes data into the memory unit and forms the service characters of the data unit, a phase device to determine the beginning point of phasing and to establish phasing modes (the synchronous method of transmission is used), pulse shaping control and reverse channel signal devices and so on.

On the other hand, if the user station only receives data, the set of equipment includes only an Akkord-12 PM receiver which operates in the telephone, data receiving and internal modes. The receiver includes a decoding unit that detects errors in the block of data received, a phasing unit, an input register designed to convert data from series to parallel code, a control pulse and reverse channel signal shaper and other equipment.

The Akkord-1200 has a memory unit for simultaneous storage of two data blocks and a modem-1200 that converts digital signals received from terminal equipment to frequency-modulated signals suitable for transmission by telephone channels and for inverse conversions.

The Minsk-1500 automatic data transmission equipment also transmits by telephone channels, but it has the capability of being directly connected to the Minsk-22 computer. An inverse code is used in the equipment to protect against errors; the reliability of transmission is 10^{-6}.

The DFE-550 automatic data transmission equipment (East German) is also used to transmit data by telephone channels at speeds of 600 and 1,200 bauds and employs cyclic codes which provide a data transmission reliability of 10^{-6}.

The information read from the punched tape is fed to the memory unit, designed to store data until it has been verified at the receiving station, and to the coding unit where the data is converted from parallel to series code, and cyclic coding operations are performed.

The information is then fed to the modem where it is converted so that it can be transmitted by telephone channels.

When information is received from communications channels, inverse conversion takes place in the modem in order to emit DC pulses to the equipment. Information is converted to parallel code by a converter that is included in the decoding unit. The information is then fed to the memory unit, to that zone in which it was located on the transmitting side. Then the correctness of the transmission is checked and if so, a confirmation signal is sent to the transmitting party by the feedback channel. If the transmission was incorrect, a signal to repeat is sent.

In view of their differences in information coding, speed of input-output from the computer and transmission by communications channels, shape of signals and so on, it is necessary to match parameters to operate data transmission and computers together. One of the methods for this assumes the use of papertape, which ensures a fuller load on communications channels because the papertape can be prepared throughout the working day, while it is transmitted only at a strictly determined time. But with this technique instantaneous data processing is impossible. Therefore, a different technique of matching the computer and communications channel is better that requires the use of special integration devices such as the Minsk-1560. This device can connect up to 32 telegraph channels with a transmission speed of 50 bauds in each line to a Minsk-32 or Minsk-23 computer, the use of unswitched telegraph lines (in this case the number of user stations cannot exceed 32) and connection by four telephone lines through Akkord-1200 or the Minsk-1500 data transmission equipment.

The Minsk-1560 device also locks out all communications lines when there is a malfunction in the computer and any particular line while it is operating or in the absence of lines. The Minsk-1560 includes line equipment, the memory unit, a control device, a calling device, a page-printing telegraph and so on.

When data is being entered from telegraph channels, it is first fed to the individual line equipment in which the telegraph messages are converted into pulse signals and then to the memory unit and shift register where the series code is converted to parallel code. The data are then fed through the exchange registers to the magnetic core storage of the computer to the address indicated in the appropriate duty register. A region of the magnetic core storage and duty register correspond to each of the 32 communications lines.

When data is being retrieved from the computer, an evenness check is made in the exchange register and it is converted from parallel code to series code in the shift register. The telegraph messages are formed by an electronic relay.

All input-output operations are coordinated by a special input-output subroutine entered in the computer in advance.

Besides the above communications equipment, communications systems and computer networks must in practice include various switching devices, from very simple electromechanical to switching centers that use electronic equipment.

The first message-switching devices were developed for telegraphy, where a rotating 360-degree selector was used as a switching element to connect users.

The brush of the selector in such a commutator moved across a contact field and was connected to the user line through a plug selector.

With the invention of the telephone and the spread of telephone communications, manually operated switchboards appeared, followed by automatic switchboards, including step-type and circular selector switchboards. The further development of switching equipment led to coordinate selectors and matrix-type relay systems. In recent years semiconductor components have begun to be used in place of relays in the connecting assemblies, which has led to the establishment of electronic switching centers.

Figure 11.5 presents a block-diagram of a communications switching center used in a computer network, which includes the following: a line equipment unit, a input-output unit, a connecting component unit, storage device and a control unit.

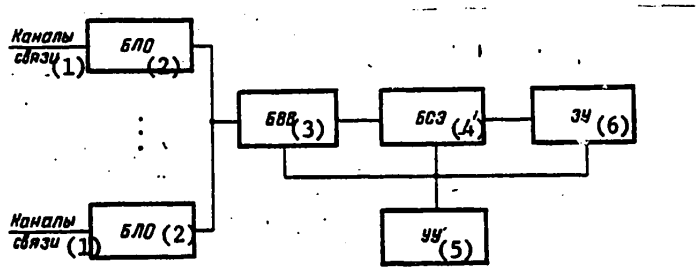

Figure 11.5. Block Diagram of Communications Switching Center

Key:
1. Communications channels
2. Line equipment unit
3. Input-output unit
4. Connecting component unit
5. Control unit
6. Storage device

The line equipment unit integrates the communications channels by means of which remote users are connected to a specific switching center. While performing this function, the block constantly monitors the status of the communications channels so that when a request is received from a user to establish communications, the necessary line can be connected, the signal decoded correctly and communications stopped at the end of the transmission. Each unit corresponds to a specific line and includes the equipment assigned to that line. Modems are installed in the line equipment unit to convert input and output signals into forms suitable for internal switching at the switching center and for transmission by communications lines.

The input-output unit is designed to identify and assign service characters (start and stop messages, tags for the beginning and end of messages and so on), verify that the equipment is connected correctly to the beginning, determine the address of the preceding switching center and perform various other functions.

The connecting component unit carries the primary load of establishing communications between users. This unit is the most important and has the greatest specific weight at channel switching centers. The principle function of the connecting components is to ensure rapid, good communications between input and output user lines. One of the methods of connection is time-sharing (spatial switching, switching physically distinct circuits) where the coordinated structure of the switching field is a matrix formed of intersection points between input and output lines.

The configuration of the switching field may vary. Thus, the number of connecting assemblies in a switching field constructed on a single-stage noninterlocking scheme (Figure 11.6a) is equal to the product of the number of input and output lines. For systems with up to 1,000 inputs and outputs, the most widespread system is the three-stage scheme (Figure 11.6b), which ensures a minimum number of connections with low probability of losing the call.

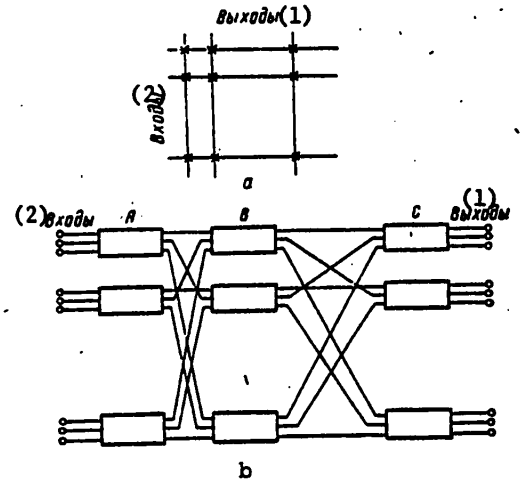

Figure 11.6. Switching Field Structures

Key:
1. Outputs
2. Inputs

When designing a communications center, an effort should be made to minimize the number of points through which the connecting path travels and ensure that the probability of interlocking is insignificant.

The storage device may be small memory units in the form of registers (chiefly in the central switching channel) designed to store information for the time required to process the call and to form the connecting channel, to store data on bypass routes and to store the various types of tables and references necessary to select routes and distribute messages. The memory of the switching centers may be organized by using large-capacity memory units, which is more typical of message-switching centers. In this case several alternatives are

possible for using the memory unit. According to one of them, two memory units are installed--one is located at the input of the message-switching center and the other at its output. Upon receipt, incoming messages are written into the first memory unit until a sufficient number of them have been collected to organize switching or until the end of the message signal is received. After this they are rewritten into the input memory units. Output to the communications channel occurs either as the messages come in on the "first received, first served" principle or according to their priority.

Another alternative assumes the existence of one memory unit that stores all information. When a signal is received that indicates the necessity to switch to message processing (verify the correctness of receiving, extract service information and so on), the output channel is checked to see whether it is occupied. After all these operations are performed and the initial channel is free, the data are fed to the communications channel. This procedure, which is the most popular today, found application in practice only after the appearance of magnetic tape, drum and disk memory units.

The control unit coordinates the work of all the units of the switching center. Thus, the initial call sent by the user is received by the control unit, which assigns the sequence of performing the operations by which the line equipment unit will scan and identify the line on which the call came, analyze all possible directions of further message travel upon finding a free path, send instructions to the connecting component unit to make the required connection and so on.

In computer networks, communications processors, concentrators and one or several computers can be connected to the switching centers. This equipment is used for partial message processing, route selection and certain other operations.

The American IBM 5910 system can be cited as an example of a message-switching center. Up to 480 telegraph channels can be connected to it through line unit 5974. The system has paired 5978 processors, one of which is in working condition and the other in reserve at any moment of time. The memory unit is composed of paired magnetic disks. The duplication of equipment included in this system provides high operating reliability. With an average message length of 300 characters, the switching device processes up to five messages per second. The message-switching center is connected to the computer through a standard IBM selector channel.

Chapter 12. YeS Remote Data Transmission System

12.1. General Information

Remote data processing systems, which are one of the foundations of computer networks, are used primarily:

for data gathering--data read from an intermediate medium at user stations is transmitted to the computer or entered directly to the computer, eliminating the need for writing to an intermediate carrier. Data input operations at the user station are practically nonexistent;

for issuing reference information--the computer processes a request received from a user station and sends the response to the station. In this case the volume of information being retrieved usually exceeds the volume of information entered;

for solving message-switching problems--data is entered from one user station and retrieved to another station virtually without processing;

for computer control when the user station is employed as a computer operator console, and also for solving many other problems.

We will consider all the questions of remote processing using the example of the YeS remote data transmission system, where such systems as the YeS-7920, YeSTEL and others have already been developed. This system includes various devices and general-purpose programs, standardized control algorithms and procedures, protocols that indicate the functional principles of different components of the system and also interfaces that define the conditions and parameters of integrating remote data processing equipment.

The chief method of control in the YeS remote data processing system is the binary-synchronous method, which assumes fulfillment of the following procedures:

establishing and maintaining synchronization in the data unit by means of synchronizing symbols which may be included in any sequence of information symbols and also transmitted without them. These symbols are removed from messages received at the receiving station. Synchronization has three phases: the bit phase, which is intended to synchronize the signal conversion units, the initial symbol phase, in which at least two synchronizing signals are sent and which is done after establishing bit synchronization but before the beginning of transmission of each block of data, and the phase of maintaining symbol synchronization, where two synchronizing symbols are entered in the information flow each second during the data transmission process;

determining the readinss of the data unit. After the synchronization procedure, the transmitting and receiving stations exchange synchronizing symbols in each direction. At the appearance of the first binary combination that differs from this symbol, the synchronization "time-out" is switched on. Upon its completion, either the synchronization procedure is repeated or one of the three following procedures is performed: set the datalink in a multipoint link, identify the station on communications channels to be switched or request receipt of data on segregated channels--data transmission in the primary mode. The last procedure begins after the data link is established. Transmission is carried out primarily in blocks using resolving feedback;

completion of data transmission. This procedure is performed when the signal for "end of transmission" is sent.

Figure 12.1 shows a block diagram of a simplified YeS remote data processing system. The integration devices in it are data transmission multiplexers which have connections, on the one hand, to the computer input-output channel

and, on the other hand, to the user station through communications equipment. The data transmission multiplexer can be connected to the user station permanently by means of unswitched (segregated) communications channels or temporarily using switched channels.

The data transmission multiplexer can be connected to one user station (single-point connection) or several (multipoint connection).

The types of channels used and the types of connections have a significant influence on the processes of establishing and breaking contact between data transmission multiplexers and user stations. Thus, with multipoint connection on segregated channels the multiplexer contact with the user station is established by sending special inquiry signals in the communications channel. When working on switched channels, contact is established by dialling the number of the desired user stations or computers depending on who is initiating the connection.

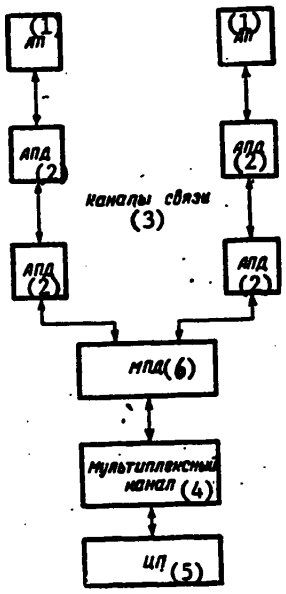

Figure 12.1. Block Diagram of Simplified Remote Data Processing System

Key:
1. User station
2. Data transmission unit
3. Communications channels
4. Multiplex channel
5. Central processor
6. Data transmission multiplexer

The YeS remote data processing system uses the five-element MTK-2 code for operation on telegraph channels and the seven-element KOI-7 code developed on the basis of the MTK-5 code for connections on telephone and wideband communications channels. Information is translated from KOI-8 and DKOI internal

machine codes to transmission codes partly by the software and partly by the hardware of the data processing multiplexer.

The YeS remote data processing system has two types of devices: hardware and software.

All the remote data processing software interacts closely with the general computer software and operates under its control.

The software, its structure and the scope of functions performed depend on the configuration of the remote processing system and on the task it is performing. Moreover, they are oriented to particular models of computers and types of peripheral equipment.

Remote data processing software is subdivided into applied program packs that expand the capabilities of the operating systems and the basic software, which facilitates the work of remote processing units and permits users to write programs in symbolic programming language.

The main components of the basic software are the basic telecommunications access method (BTMD) and the general telecommunications access method (OTMD), which is achieved in the operating system and disk operating system of the YeS computer and ensures the establishment of communication with the user station, detection and correction of errors, control of the buffer memory, data conversion and so on. It is more difficult to achieve the basic telecommunications access method because it requires that the user, when writing programs, have a detailed knowledge of the technical specifications and composition of data input-output equipment at the user station and that he also be thoroughly familiar with methods and modes of data transmission. The user himself must include the addresses of user stations and the inquiry sequence in the programs and perform many other additional functions.

Since the general telecommunications access method essentially precludes any effect of the remote data processing hardware specifications, this method provides a higher level of software than the basic telecommunications access method. It performs all the functions of the basic method and also edits message titles, controls the organization of queues, establishes modes of interaction between the computer and the user station and so on. The general telecommunications access method has been achieved in the operating system of the Unified Computer System and is used chiefly in high-level remote data processing systems.

12.2. Remote Data Processing Hardware

Remote data processing hardware includes data transmission equipment by which the data processing equipment is connected to the communications network, devices to integrate the computer and the data transmission equipment to ensure control of data exchange, matching of electrical signals and speeds and so on and user stations with various types of peripheral equipment. Figure 12.2 shows the classification of hardware used in the YeS remote data processing system.

The data transmission equipment makes it possible to work with both switched and segregated telegraph and telephone channels as well as wideband communications channels and physical lines.

Signal conversion devices, error-protection devices and automatic call devices are included among the data transmission equipment of the YeS system, as well as other data transmission equipment.

The most widely used of these devices are signal conversion units. They are in turn subdivided into the following:

modems which convert digital binary signals from a computer or user station to signals that can be sent by telephone or wideband communications channels and perform the inverse conversion;

signal conversion devices for telegraph communications used for operating on telegraph lines to raise the level of the logic signal and its output;

signal conversion devices for connecting lines to transmit data over distances up to 10-14 kilometers by connecting lines. The most widely used are low-level data conversion devices which convert digital signals to low-level DC signals, which minimizes the insignificant mutual effect of signals of different circuits.

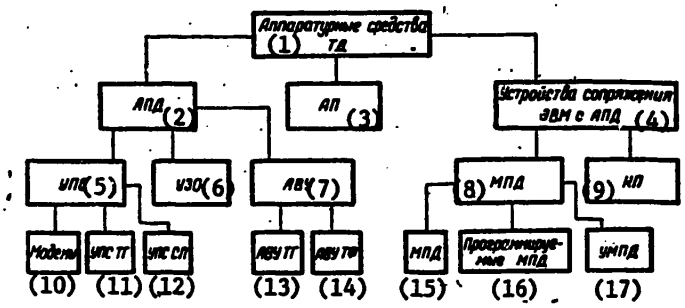

Figure 12.2. Classification of Remote Data Processing Hardware

Key;

1. Remote data processing hardware
2. Data transmission equipment
3. User station
4. Computer-data transmission equipment integration devices
5. Signal conversion devices
6. Error-protection devices
7. Automatic call devices
8. Data transmission multiplexers
9. Communications processors
10. Modems
11. Signal conversion devices for telegraph channels
12. Signal conversion devices for connecting lines
13. Automatic call devices for telegraph lines
14. Automatic call devices for telephone lines
15. Data transmission multiplexers
16. Programmable data transmission multiplexers
17. Remote data transmission multiplexer

The specifications of the various signal conversion devices developed for the YeS remote data transmission systems are shown in Table 12.1.

Error-protection devices encode and decode messages and detect errors in them. They use matrix or cyclic codes which have the polynomials $x^{16} + x^{12} + x^5 + 1$ or $x^{24} + x^{23} + x^7 + x^5 + x^2 + 1$. Error-protection devices with high-level codes are used in cases which require very high data transmission accuracy and communicate in only a few directions. The presence of an error-protection unit considerably increases the cost of building a remote data transmission system and makes construction more complicated. In most cases, however, the required transmission reliability is achieved either by computer programs or by the hardware and software of the user station. Table 12.2 presents the specifications of error protection devices related to the YeS remote data processing system.

The UZO-4800 is designed to work with user stations not included in the nomenclature of the Unified Computer System, while the UZO-48000 is for intercomputer data exchange and the UZO-2400 is for working with AP-2 and AP-3 user stations.

The automatic call devices (AZU) automate the establishment of connections in switched networks and are subdivided into units designed to work on telegraph (YeS-8063) and telephone (YeS-8061 and YeS-8062) communications channels.

The following standards for unified interfaces have been established in the YeS remote data transmission system to standardize the integration of specific units: S1 junction for signal conversion devices to communications channels, S2 junction for signal conversion devices and automatic call devices to data processing equipment and S3 junction for error-protection units to data processing equipment.

Devices to integrate computers and data transmission equipment consists of data transmission multiplexers and communications processors.

The data transmission multiplexers are the central units of the remote data processing system and determine its capabilities and configurations. These units provide: interaction between the computer and the user station through communications channels, with essential data conversion, partial buffering (the main computer memory is used for complete buffering), interference-stabilizing coding and so on;

execution of data control algorithms that are achieved for each user station and that contain procedures to establish and break the data link, for identification and inquiry and for data transmission. The order of fulfilling the procedures is initiated in the data transmission multiplexer by a sequence of channel programs and instructions;

control of data transmission channels and equipment, i.e., logic and electrical integration of the computer and the data transmission equipment are achieved.

Table 12.1. Specifications of Signal Conversion Devices

Model	Number	Manufacturing Country	Transmission Mode	Type of Transmission	Transmission Speed, bauds	Type of Communications Channel	Modulation
Modem-200	YeS-8001	Soviet Union, Bulgaria	Duplex	Synchronous, asynchronous	200	Switched and Segregated Telephone	Frequency
Modem-200	YeS-8002	East Germany, Hungary, Czecho-slovakia	Duplex, semi-duplex	Asynchronous	200	" "	"
Modem-1200	YeS-8005	Bulgaria	Semiduplex	Synchronous, asynchronous	600, 1,200	" "	"
Modem-2400	YeS-8010	Soviet Union	Duplex	Synchronous	600, 1,200 2,400	Segregated Telephone	Double Relative Phase
Modem-2400	YeS-8011	Hungary	Duplex, semi-duplex	" "	1,200, 2,400	" "	"
Modem-4800	YeS-8015	Soviet Union	Duplex	" "	2,400, 4,800	" "	Triple Relative Phase
Modem-48000	YeS-8019	Soviet Union	Duplex	" "	24,000, 48,000	Wideband	Bipolar Amplitude
Low-Level Signal Conversion Unit	YeS-8027	Bulgaria	Duplex, semi-duplex	Synchronous, asynchronous	50, 100, 200, 600, 1,200	Physical Line	-
Low-Level Signal Conversion Unit	YeS-8029	Soviet Union	"	" "	96,000	" "	-

[Table continued on following page]

Table 12.1 [Continued from preceding page].

Telegraph Signal Conversion Unit	YeS-8030	Bulgaria	"	"	50, 100, 200	Segregated Telephone	-
Telegraph Signal Conversion Unit	YeS-8032	Czechoslovakia	"	"	"	Segregated and Switched Telephone	-

The YeS remote data transmission system assumes several types of data transmission multiplexers that differ by the number and variety of units of data transmission equipment, user stations and communications channels. The computer in all data transmission multiplexers is connected to the multiplex channel and the structure is similar, consisting of a computer input-output channel integration device which performs parallel data exchange between the data transmission multiplexer and the computer, a two-channel switch that permits operation with two multiplex channels and different models of YeS computers and line adapters that take into account the special characteristics of user stations that are being connected. The number and composition of line adapters depend on the type of data transmission multiplexer and the configuration of the remote data processing system.

Table 12.3 presents the specifications of data transmission multiplexers that have been achieved with the YeS remote data transmission system. All the multiplexers are connected to the multiplex channel of the computer through a standard input-output interface; they are connected to the data transmission equipment through an S2 junction and directly to telephone channels through an S1 junction.

The MPD-1A (YeS-8400) data transmission multiplexer permits up to 15 different user stations to be connected to the computer through communications channels. These stations can be the AP-61, AP-63, AP-70, RTA and any model of the YeS computer which includes an MPD-1A. The transmission speed over physical lines and telegraph communications channels is 75 bauds; it is 200-4,800 bauds over telephone channels.

Telegraph communications channels and physical lines are connected to the multiplexer either separately or through a signal conversion unit; telephone channels are connected by a Modem-200 or Modem-2400. All incoming and outgoing connections are automatic. The only exception is establishing outgoing connections on switched telegraph lines. This operation is performed at the in tiative of the computer by the operator, who manually dials the number retrieved by the computer.

The following line adapters have been developed for the MPD-1A: AD1 for working with page-printing telegraphs through switched telegraph communications channels, the AD-2 for working with the AP-70 through segregated telegraph channels, the AD-3 for working with the AP-61 and AP-63 through the Modem-2400 and segregated telephone channels and the AD-4 for working with the AP-1 and AP-70 through telephone channels and the Modem-200. These adapters provide a semiduplex data exchange mode. The AD-5 adapter communicates between models of YeS computers in the duplex mode. The AD-6 synchronous adapter is used for working with all synchronous user stations on unswitched telegraph lines. The MPD-1A has an adapter connection unit (BPA) for connecting the line adapters that communicate with the channel integration unit and an adapter synchronization unit (BSkhA) for control of the adapters.

Figure 12.3 shows one possible configuration when using the MPD-1A.

Table 12.2. Specifications of Error Protection Devices

Model	Code of Device	Manufacturing Country	Transmission Speed, bauds	Code	Error Protection Method	Transmission Mode	Type of Communications Channel	Method of Connection to Channel
UZO-1200	YeS-8121	USSR	600, 1,200	MTK-5	Cyclic with Polynomial $x^{16}+x^{12}+x^5+1$	Semiduplex	Telephone	Through Modem-1200
UZO-2400	YeS-8122	Hungary	200, 600, 1,200, 1,400	KOI-7	Cyclic with Repetition	Duplex	Telegraph	Through MTD-1
UZO-4800	YeS-8135	USSR	50, 100, 200, 2,400, 4,800	KOI-8	Cyclic with Polynomial $x^{16}+x^{12}+x^5+1$	Duplex	Segregated Telephone	Through Modem-2400
UZO-48000	Yes-8140	USSR	24,000, 48,000	MTK-5 or KOI-8	Cyclic with Polynomial $x^{24}+x^{23}+x^7+x^2+1$	Duplex	Broad-Band	Through Modem-48000

Table 12.3. Specifications of Data Transmission Multiplexers

Model	Code	Manufacturing Country	Number of Connected User Stations	Type of User Station	Transmission Speed, bauds	Method of Error Protection
MPD-1A	YeS-8400	USSR	15	AP-1; AP-61; AP-62; AP-63; AP-64; AP-70, and others; MPD-1A, telegraph	75, 4,800	Matrix and cyclic code
MPD-2	YeS-8402	USSR	8-176	AP-1; AP-2; AP-4; AP-14; AP-31; AP-50; AP-61; AP-63, and others; MPD-2, telegraph	50, 4,800	Linear-Transverse "Verification" and Cyclic Code
MPD-3	YeS-8403	USSR	4	AP-1; AP-2; AP-3; AP-4; AP-70; MPD-3, and others, telegraph	50, 4,800	" "
MPD-1	YeS-8401	Bulgaria	32-64	AP-1; AP-31; AP-61; AP-62; AP-70; MPD-1, and others, telegraph	50, 2,400	-
MPD-4	YeS-8404	East Germany	12	AP-1; AP-5; AP-6; AP-62; AP-70	20-1,200	Matrix Code
UMPD	YeS-8421	Hungary	20	AP-1; AP-62; AP-64, and others; MPD, telegraph	50-200	-

The MPD-3 (YeS-8403) data transmission multiplexer provides communications between the YeS-1020, YeS-1030, YeS-1050 and YeS-1060 computers with four user stations, as which the AP-1, AP-3, AP-11, AP-70 and the page-printing telegraph or the YeS computer with the MPD-3 can be used.

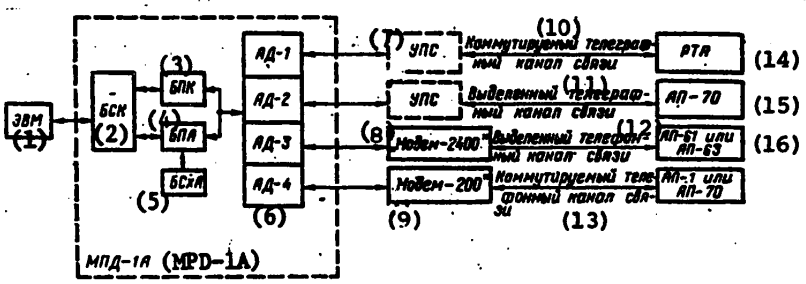

Figure 12.3. Configuration of YeS Remote Data Processing System Using MPD-1A

Key:

1. Computer
2. Input-output channel-computer integration unit
3. Channel integration unit
4. Adapter connection unit
5. Adapter synchronization unit
6. Line adapter
7. Signal conversion device
8. Modem-2400
9. Modem-200
10. Switched telegraph communications channel
11. Segregated telegraph communications channel
12. Segregated telephone communications channel
13. Switched telephone communications channel
14. Page-printing telegraph
15. User station
16. Or

The described multiplexer has the following types of line adapters:

TA-1 start-stop adapter by which the AP-1 and AP-70 user stations are connected to the MPD-3 over switched and segregated telephone channels through the Modem-200 and AVU-TF automatic call device;

TA-2 start-stop adapter that facilitates communications of the MPD-3 over segregated telegraph channels with user stations in which telegraph equipment has been installed. Only hardware control of the information being transmitted is exercised;

SA-1 synchronous adapter through which the AP-11 or similar MPD-3 are connected to the multiplexer over segregated telephone channels.

Communications is established through the Modem-2400. The error protection method is a cyclic code with generatrix of polynomial $x^{16} + x^{12} + x^5 + 1$;

AA-1 asynchronous adapter through which the UZO-1200 error protection device and the Modem-1200 connect AP-2 and AP-3 user stations to a given multiplexer over switched and segregated telephone communications channels. The reliability of the transmitted information is increased by using the error protection device.

The MPD-3 can be supplied with various types of line adapters to provide a semiduplex data exchange mode. The following line adapters--DA-1 when working with a user station not included in the Unified Computer System and DA-2 that supports intercomputer exchange--are used to operate in the duplex mode. Information is transmitted over communications channels at speeds of 50-4,800 bauds. The configuration of the remote data transmission system using the MPD-3 is shown in Figure 12.4.

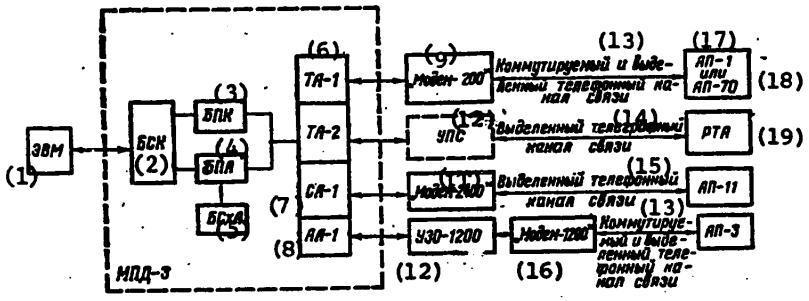

Figure 12.4. Configuration of YeS Remote Data Processing System Using MPD-3

Key:

1. Computer
2. Channel integration unit
3. Channel connection unit
4. Adapter connection unit
5. Adapter synchronization unit
6. Telegraph
7. Synchronous adapter
8. Asynchronous adapter
9. Modem-200
10. Signal conversion unit
11. Modem-2400
12. Error protection device
13. Switched and segregated telephone communications channel
14. Segregated telegraph communications channel
15. Segregated telephone communications channel
16. Modem-1200
17. User station
18. Or
19. Page-printing telegraph

The MPD-1 (YeS-8404) data transmission multiplexer provides connection of user stations over 32 (with possible increase to 64) switched and segregated telephone channels and unswitched telegraph channels, as well as on physical lines. The speed of transmission can be 50, 75, 100, 200, 600, 1,200 and 2,400 bauds.

The MPD-1 has three types of adapters--the TA-1 works with the AP-1 and AP-70 user stations through switched and unswitched telephone channels, the TA-2 works with telegraph equipment and the TA-3 operates with AP-61 and AP-63 user stations over unswitched telephone communications channels. The MPD-1 includes a memory unit containing two modules with 32 addressable cells each, which contain the line control words. One module has a capacity of 2,112 bits and is connected to TA-1 and TA-2 adapters and the other, having a capacity of 2,240 bits, is connected to the TA-3 adapter.

The MPD-2 (YeS-8402) programmable data transmission multiplexer is designed to organize large systems within the Unified Computer System. It exchanges data between computers and all types of data transmission multiplexers and user stations included in the YeS remote data processing hardware.

The MPD-2 permits connection of 8 to 176 communications lines with spacing of increasing the number of communications channels equal to eight. Unswitched and segregated telephone communications channels and physical lines can be used in this case. The transmission speeds are 50, 100, 200, 600, 1,200, 2,400 and 4,800 bauds.

Unlike the considered hardware data transmission multiplexers in which the nomenclature of the user stations is always limited, the MPD-2 permits the connection of different types of user stations. This advantage greatly increases the flexibility of the system, contributes to expansion when necessary and increases the number of connected user stations.

New user stations are connected by rewriting a program into the MPD memory without making changes in its circuitry. The MPD-2 includes a disk memory unit with capacity of 4,096 72-digit words and a microprogramming control unit. Using these devices, the multiplexer performs functions related to execution of specific exchange algorithms. Besides these devices, the MPD-2 contains an internal storage device where control and information line words are stored for all communications channels.

The YeS-8421 remote data transmission multiplexer concentrates 20 unswitched telegraph communications channels operating at a speed of 50 bauds and having user stations at the ends into a single unswitched telephone line having a speed of 1,200 bauds. The use of this multiplexer permits the number of communications channels to be considerably reduced and a significant increase of their utilization efficiency. One of the possible configurations of a remote data processing system using the remote data transmission multiplexer is shown in Figure 12.5.

Since the functions of the remote data processing system related to analysis of headings, establishment of queues, message editing and interrogation of user station status are performed by a computer, further development of the YeS remote data processing system assumes the development and introduction of special communications processors and the related redistribution of remote data processing functions.

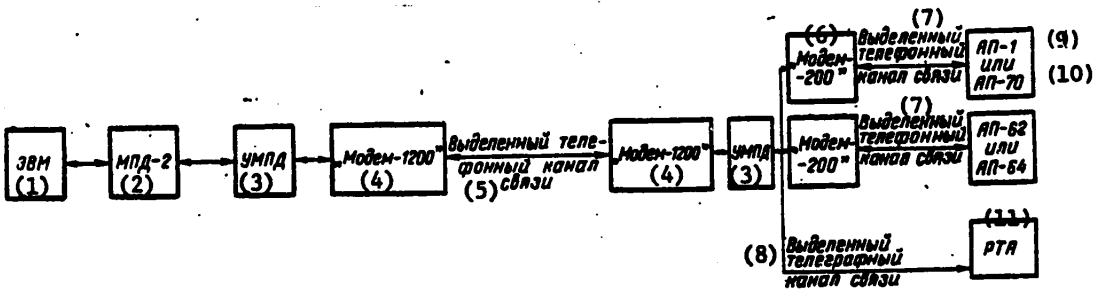

Figure 12.5. Configuration of YeS Remote Data Processing System Using Remote Data Transmission Multiplexer

Key:
1. Computer
2. MPD-2
3. Remote data transmission multiplexer
4. Modem-1200
5. Segregated telephone communications channel
6. Modem-200
7. Segregated telephone communications channel
8. Segregated telegraph communications channel
9. User station
10. Or
11. Page-printing telegraph

The use of communications processors instead of data transmission multiplexers contributes to a reduction of the computer load, an increase of the flexibility and reliability of the system and also to the capability of using them as a message-switching center in computer networks. In most cases communications processors are minicomputers supplemented with special software. Line adapters accomplish integration functions of the minicomputer to the central computer and transmission devices.

6521
CSO: 8144/0540-A

GENERAL DATA ON COMPUTER CONFIGURATION

Moscow EVM I VYCHISLITEL'NYYE SETI in Russian 1980 (signed to press 20 May 80) pp 61-67, 117-118, 122-124, 131-134, 145-148, 157-158, 224-250

[Excerpts from the book "Computers and Computer Networks" by Vasiliy Nikolayevich Kriushin, Inna Nikolayevna Buravtseva, Nina Mikhaylovna Pushkina and Nina Grigor'yevna Chernyak, Izdatel'stvo "Statistika", 18,000 copies, 328 pages]

[Excerpts] Chapter 4.

4.3. Composition and Main Characteristics of Unified Computer System and Modular Computer Equipment Systems

The unified computer system (YeS EVM) is a family of program-compatible models of third-generation computers designed to solve a wide range of scientific and technical, economic, information-logic and control problems. These machines are oriented toward their use in automated control systems.

The Unified Computer System was developed within the framework of cooperation of socialist member countries of CEMA. The first unit (Ryad-1) of the Unified Computer System includes several models produced in large series (Table 4.1). Industrial production of the first machines of the Unified System was begun in 1972.

Table 4.1.

Models of Unified Computer System	Developing Country
YeS-1010	Hungarian Peoples Republic
YeS-1020	USSR and Peoples Republic of Bulgaria
YeS-1021	CSSR
YeS-1022	USSR
YeS-1030	USSR and Polish Peoples Republic
YeS-1032	Polish Peoples Republic
YeS-1033	USSR
YeS-1040	German Democratic Republic
YeS-1050	USSR

The computer hardware of the Unified System includes processors with different speed, selector and multiplex channels, an aggregate of standard interfaces

between channels and the control devices of external devices and a large nomenclature of peripheral devices of different designation (see Figure 4.2).

The main features of the computers of the Unified system are:

program compatability "from bottom to top" of individual computer models that ensures the succession of programs when switching from one model to another;

standard integration of external devices with input-output channels that permits a large number of different external devices to be connected;

capability of combining several computers into a single system;

capability of operating in control systems in real time

Standardization and unification provided by a system of standards became necessary when developing the Unified Computer System. The system of standards or system of normative and technical documents of the Unified Computer System is understood as the complex of interrelated standards that establish the aggregate of the norms, regulations and requirements, fulfillment of which determines the modular design of computer models of the Unified System. For example, state standards on computer equipment (GOST 16325-76 "General-Purpose Computers. General Specifications") establish six classes in productivity for a family of computers, determining for each class the lowest capacity of the internal storage devices and the functions performed by the computer. The models of the Unified Computer System can be divided into classes as shown in Figure 4.3.

The main characteristics of the computers of the Unified System (the Ryad-1) are presented in Table 4.2.

Each of the models of the Unified Computer System has (compulsory) a minimum standard complement of hardware adequate for functioning of the corresponding operating system. The minimum composition of the equipment of the first unit of computers of the Unified System is presented in Table 4.3.

The principles on which the family of the Unified Computer System was developed permit the capability of each of the computers to be expanded by increasing the internal storage capacity, increasing the number and changing the nomenclature of external devices and connection of a second processor. Program and information compatibility are fully retained on expansion.

Auxiliary functional devices contribute to an increase of system productivity, orientation toward specific areas of application and to providing increased operating requirements.

The combination of hardware and software of the Unified Computer System ensures operation in all modes usually required by users: batch processing, multiprogram, real-time, dialogue and time-sharing.

The models of the Ryad-2 Unified Computer System include the following: YeS-1015 (Hungarian Peoples Republic), YeS-1025 (CSSR), YeS-1035 (CSSR) and Peoples Republic

Characteristics	Class of Computer 1	2	3	4	5	6
Models of Unified Computer System	1010	1020	1030 1022 1025 1040	1033 1035 1050	1060 1055	1065
Productivity (instructions/s)	To 10^4	From 10^4 to $5 \cdot 10^4$	From $5 \cdot 10^4$ to $5 \cdot 10^5$	From $5 \cdot 10^5$ to 10^6	From 10^6 to $2 \cdot 10^7$	more than $2 \cdot 10^7$
Main storage capacity (Kbytes/not less than)	64	128	256	512	2,048	8,192
Multiprogram operation	-	+	+	+	+	+
Time-sharing operation	-	-	-	+	+	+
Real-time operation	-	-	-	+	+	+
Local and/or remote batch processing	+	+	+	+	+	+
Capability of working with user stations through communications lines	+	+	+	+	+	+
Capability of organizing multiprocessor systems	-	-	-	+	+	+
Capability of organizing multimachine systems	+	+	+	+	+	+

\+ Compulsory requirement
\- Optional requirement

Figure 4.3. Characteristics of Types of Computers

Table 4.2. Main Characteristics of Computer Models of Unified System (Ryad-1) Produced in the USSR

Main Characteristics \ Computer Models	YeS-1020	YeS-1030	YeS-1050	YeS-1022	YeS-1033
Productivity, thousand ops/s	20	100	500	80	200
Internal storage capacity, Kbytes	64-256	128-512	256-1,024	128-512	256-512
Magnetic disk storage					
pack capacity, Mbytes	7.25	7.25	7.25	7.25	7.25
speed, Kbytes/s	156	156	156	156	156
Magnetic tape storage					
maximum speed, lines/s	64,000	96,000	96,000	64,000	64,000
recording density, lines/mm	8/32	8/32	8/32	8/32	8/32
Multiplex channel transmission speed, Kbytes/s:					
in monopole mode	100	300	180	300	350
in multiplex mode	10-16	40	110	40	70
Selector channel transmission speed, Kbytes/s	300	800	1,300	500	800

Table 4.3. Basic Composition of Models of Unified Computer System (Ryad-1) Produced in the USSR

Unified Computer System Hardware-	YeS-1020		YeS-1030		YeS-1050		YeS-1022		YeS-1033	
	Code	Number	Code	Number	Code	Number	Code	Number	Code	Number
Processor	YeS-2020	1	YeS-2030	1	YeS-2050	1	YeS-2622	1	YeS-2433	1
Internal storage	YeS-3220	1	YeS-3203	1	YeS-3205	2	YeS-3222	1	YeS-3207	1
Channels:										
multiplex	In pro-		YeS-4430	1	YeS-4012	1	In pro-			
	cessor						cessor			
	"		YeS-4430	3	YeS-4035	2	"			
selector										
Magnetic disk storage (NMD)	YeS-5056	2	YeS-5056	2	YeS-5050	5	YeS-5056	2	YeS-5056	4
Magnetic tape storage (NML)	YeS-5010	4	YeS-5019	4	YeS-5019	8	YeS-5017	4	YeS-5017	4
Control devices:										
magnetic disk	YeS-5551	1	YeS-5551	1	YeS-5551	1	YeS-5551	1	YeS-5551	1
magnetic tape	YeS-5511	1	YeS-5511	1	YeS-5511	1	YeS-5517	1	YeS-5517	1
Input devices:										
punch card	YeS-6012	1	YeS-6012	1	YeS-6013	2	YeS-6012	1	YeS-6012	1
papertape	YeS-6022	1	YeS-6022	1	YeS-6022	1	YeS-6022	1	YeS-6022	1
Output devices:										
punch card	YeS-7010	1	YeS-7010	1	YeS-7012	1	YeS-7012	1	YeS-7010	1
papertape	YeS-7022	1	YeS-7022	1	YeS-7022	1	YeS-7022	1	YeS-7022	1
Typewriter	YeS-7070	1	YeS-7070	1	YeS-7077	2	YeS-7077	1	YeS-7077	1
Data preparation devices:										
punch card	YeS-9010	2	YeS-9010	2	YeS-9010	1	YeS-9010	1	YeS-9010	2
papertape	YeS-9020	2	YeS-9020	2	YeS-9020	1	YeS-9020	1	YeS-9010	2
Alphanumeric and graphic screen console	---	-	---	-	YeS-7064	1	---	-	---	-

of Bulgaria), YeS-1045 (USSR and Polish Peoples Republic), YeS-1055 (GDR), YeS-1060 (USSR) and YeS-1065 (USSR) [17].

The main specifications of models of the Ryad-2 Unified Computer System are presented in Table 4.4.

Table 4.4. Main Characteristics of Ryad-2 Models of the Unified Computer System Developed in the USSR

Computer Code	Producing Country	Productivity thousand ops/s	Storage Capacity, Kbytes
YeS-1035	USSR, Peoples Republic of Bulgaria	140- 160	256- 1,024
YeS-1045	USSR, Polish Peoples Republic	540- 880	1,024- 4,096
YeS-1060	USSR	1,300-1,600	1,024- 8,192
YeS-1065	USSR	4,000-5,000	2,048-16,324

These models retain the program compatibility with Ryad-1 computers of the Unified System. The main difference of Ryad-2 models includes a new component base--large integrated circuits, an increase of speed, an increase of storage capacity, greater reliability and significant expansion of functional capabilities (dynamic memory distribution, complexing of models and multiprocessor systems and so on).

The modular computer equipment system (ASVT) was developed to solve problems of preliminary processing of economic information, calculation of engineering and economic indicators, processing information in information-measuring systems and centralized monitoring systems and control of production facilities. The ASVT is a set of modular devices with unified external communications, from which different computer systems with given technical parameters can be configured, beginning with the simplest information gathering systems and ending with complex multiprocessor data processing systems.

The complete set of communications-standardized units and devices permits one to take into account the most diverse requirements of control systems and to develop complexes that have satisfactory redundancy from the user's viewpoint. The characteristic feature of ASVT is that their specifications can be varied over a wide range when developing different systems. Moreover, the modular system permits gradual modernization by replacing individual devices by more modern devices.

Equipment redundancy due to standardization of functional communications units is repaid by serial production of a computer equipment system.

ASVT can be divided into six groups according to functional designation of the device:

central control and information processing devices--processors;

information storage devices--internal and external storage devices;

facility-communications devices, the complete nomenclature of which ensures information communications of the computer system designed on the basis of ASVT with any of the sensors and servomechanisms serially produced in the USSR;

personnel communications devices of the operational production control system, information carrier input devices and output devices;

extrasystems communications line output devices (telegraph, telephone, radio relay and so on);

intrasystems communications devices that provide information exchange between modular devices within the system.

The second unit of the ASVT (ASVT-M) was designed on a microelectronics base (integrated circuits) and permits development of complexes of machines and devices of different classes and also has the capability of communicating with the Unified Computer System.

The ASVT-M contains M40 and M6010 automatic microprogram devices, M400, M5000, M5010, M6000, M7000 and M4030 digital computers, a large number of external systems devices, facility-communications devices and digital and graphic information display devices.

Models M40, M400, M6000, M7000 and M6010 have highly effective devices for communicating with control facilities and are usually employed in production process control systems, scientific experiment automation systems and so on. These machines operate primarily in real time.

Models M4030, M5000 and M5010 are characterized by higher productivity compared to earlier produced models, an extensive instruction system and the presence of alphanumeric processing devices. They are also designed to operate in real time and in this case communications with sensors are most frequently carried out through low-level systems designed on the basis of M40, M6000, M7000 and M6010 computer complexes.

ASVT-M devices permit multimachine complexes to be constructed from computers of different classes, for example, M4030 computers of the SM EVM [International Small Computer System]. The most productive complex of the ASVT-M is the M4030 computer complex. The M4030 complex is called upon to comprise the technical base of ASU in combination with devices and automatic equipment of other modular complexes of the state instrument system (GSP). The M4030 provides the capability of realizing multimachine hierarchical control systems based on models different in productivity and designation and contained in the ASVT-M.

The M4030 model is designed for use as a central machine:

in the ASUP [Automated production control system] to solve a complex of problems (control of production, optimum organization of it, engineering and economic planning, bookkeeping and accounting and so on);

production process ASU (together with the International Small Computer System);

in scientific and physical experiment automation systems and so on.

The configuration, equipment and software system of the M4030 model ensure its compatibility with the Unified Computer System in instructions, data format, internal codes, interface and user programs in assembler and high-level languages having translators in the DOS (disk operating system) of the Unified Computer System and the DOS of the ASVT.

The processor of the M4030 model has the universal instruction system of the ASVT and the Unified Computer System expanded by introducing auxiliary transmission instructions, comparison of large information files and shifting and rounding off decimal operands. The average productivity of the processor (according to Gibson) is 100,000 operations per second.

The internal storage has capacity of 128-512 Kbytes and cycle time is 2 microseconds.

The input-output devices and external stores are connected to the processor by three selector and one multiplex channels. The multiplex channel transmits data in the monopole mode at a speed of 140,000 bytes per second and in the multiplex mode at a speed of 50,000 bytes per second. The selector channel has maximum data transmission speed of one million bytes per second.

The M4030 contains a standard set of peripheral devices: magnetic tape and magnetic disk external storage, punch card and papertape input devices, printout, punch card and papertape devices and displays.

The processor of the M6000 model is the minimum baseline configuration of the computer complex configured from modules (57 types) and 15 different complexes can be developed on its basis depending on the sphere of application [2].

Computer Storage Devices

Table 6.1. Internal Storage Devices (OZU)

Computer	Storage Device Code	Cycle Time, μs	Capacity, Kbytes	Digit Capacity, bytes
YeS-1020	YeS-3220	2	64- 256	2
YeS-1022	YeS-3222	2	128- 516	4
YeS-1030	YeS-3203	1.25	128- 256	4
YeS-1033	YeS-3207	1.2	256- 512	4
YeS-1040	YeS-3204	1.35	256-1,024	8
YeS-1050	YeS-3205	1.25	256-1,024	8
BESM-6		2	64- 128**	50*
ASVT-M	A-211-8	2.5	4	2
M4030		2	128- 512	2

*Bits for the BESM-6.

**Words.

Table 6.1 (Continued).

External Storage Devices (VZU)

1. Magnetic Disk and Magnetic Drum VZU (Direct Access VZU) [4]

Type of VZU	VZU Code	Capacity, Mbytes	Data Transmission Speed, Kbytes/s
Interchangeable magnetic disk store	YeS-5050	7.25	156
Interchangeable magnetic disk store	YeS-5061	29.17	312
Interchangeable magnetic disk store	YeS-5066	100	806
Permanent magnetic disk store	YeS-5060	0.8	150
Permanent magnetic disk store	YeS-5051	125	83.25
Magnetic drum store	YeS-5033	6	1,250
Magnetic drum store	YeS-5035	2	100

2. Magnetic Tape VZU

VZU Code	Information Recording Density, bits/mm	Maximum Data Transmission Speed, Kbytes/s
YeS-5010	8/32	64
YeS-5014	63	126
YeS-5015	63	252
YeS-5016	8/32	48
YeS-5019	8/22/32	96
YeS-5022	8/32	128
YeS-5003	32/63	315

Buffer storage devices (BZU) are used to increase the efficiency of information exchange between internal and external storage devices having different speed. Buffer storage devices occupy an intermediate position in capacity and speed between OZU and VZU. Magnetic drums and disks are used as the information carriers in BZU.

Multifunctional storage devices (MFZU), that along with information storage, read and write functions, also realize logic, arithmetic and special operations on the information stored in them, have found application in third-generation computers. The following operations can be performed in MFZU: general and simple associative retrieval, code retrieval and comparison according to different number criteria, minimum and maximum word retrieval, closest minimum and maximum word retrieval, retrieval of all numbers within given limits, any set of digit and complex logic operations, arithmetic operations and so on.

The memory of the models of the Unified Computer System is organized on the hierarchical principle and has the form shown in Figure 6.4.

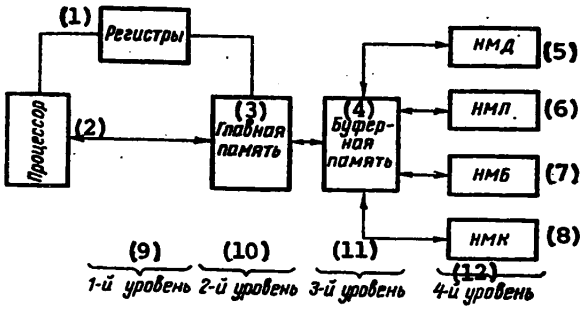

Figure 6.4. Hierarchical Structure of Storage Devices of Unified Computer System

Key:

1. Registers
2. Processor
3. Main storage
4. Buffer storage
5. Magnetic disk store
6. Magnetic tape store
7. Magnetic drum store
8. Magnetic card store
9. First level
10. Second level
11. Third level
12. Fourth level

The local memory is at the first level.

The local level of the YeS-1050 is designed on semiconductor flip-flops. The flip-flop registers have direct addressing and can be used to store operands, addresses and indexes. The total capacity of the local memory of the YeS-1050 is 864 bits and the cycle time is 160 nanoseconds.

The local memory of the YeS-1030 is an internal storage device with random access of addresses on thin cylindrical magnetic films. The capacity of the local memory is equal to 64 36-digit words and cycle time is 0.6 microseconds.

The local memory of the YeS-1020 is structurally contained in the main internal storage (OOP). Regardless of the capacity of the internal storage, that of the local memory comprises 256 bytes. The cycle time is the same as that in the OOP, i.e., 2 microseconds.

The main internal storage (OOP) is located on the second level. It is designed on the basis of ferrite cores with rectangular hysteresis loop by the 2.5D system and has capacity of 64-1,024 Kbytes with cycle of 1.25-2.0 microseconds. Simultaneous access to two internal storage units is possible in older models, i.e., so-called double stratification of the memory, which ensures higher speed.

The read-only memory used in the Unified Computer System to store control information and microprograms is also located at the second level.

The third-level storage device includes a multiplex memory in which information that controls the operation of the multiplex channel is stored. It is an independent storage device in older models of the Unified Computer System. The memory of

the multiplex channel is designed in the YeS-1030 on the basis of thin magnetic films, as is the local memory, and has a capacity of 1,024 32-bit information words with minimum cycle time of 1 microsecond.

The multiplex memory in the YeS-1050 is based on ferrite cores with wiring organized by the 2D system. The memory capacity is equal to 8 Kbytes.

The multiplex memory in the YeS-1020 is structurally contained in the main internal storage. The capacity of the multiplex memory depends on the capacity of the OOP.

The fourth-level storage device consists of magnetic drum, magnetic disk, magnetic tape and magnetic card stores. The main complex in the YeS-1020 includes only magnetic disk and magneti tape external storage devices. All types of external storage are provided in the basic complex in older models.

Composition and designation of internal storage of YeS-1020 model. The internal storage of the YeS-1020 model consists of three independent logic types of memory: internal storage (OOP), local memory (LP) and multiplex memory (MP). All types of memory are structurally arranged in a common memory unit. Access is possible only to one of the indicated types of memory at each moment of time. Register (RNZ) is used as the information register of all types of memory and register (RMN) is used as the address register. Two bytes of information are written or read in parallel code simultaneously upon access to the memory.

The main internal storage with capacity of 32 K two-byte words is located in the same magnetic unit. However, the capacity can be increased by including additional magnetic units in the computer. Depending on the modification of the internal storage, the capacity of different types of the memory corresponds to the data presented in Table 6.4.

Table 6.4.

Modification of OOP	Capacity of Memory, bytes		
	OOP	LP	MP
YeS-3200-1	64K	256	768
YeS-3220-2	128K	256	1,792
YeS-3220-3	256K	256	1,792

The total access cycle consists of two independent cycles: read and write cycle. The minimum cycle time of access to the internal storage, determined by the time between two sequential read instructions, comprises 2 microseconds. Information is read in the read cycle by the address stored in the RMN register, the read information is recorded in the RNZ register and is regenerated in the memory unit.

Information is erased in the write cycle by the address indicated in the RMN and information is then recorded from the RNZ register.

The total capacity of the internal storage is divided by the number of digits into 18 ferrite fields (16 information digits and 2 verification digits). The ferrite field of each digit is represented in the form of a rectangular matrix consisting

of 32 K cores (32 X 1,024). This matrix is divided into two parts (semimatrix) measuring 512 X 32 each. The semimatrices are structurally arranged on two sides of the plane of the magnetic unit (MB). A diagram of the magnetic unit is presented in Figure 6.9.

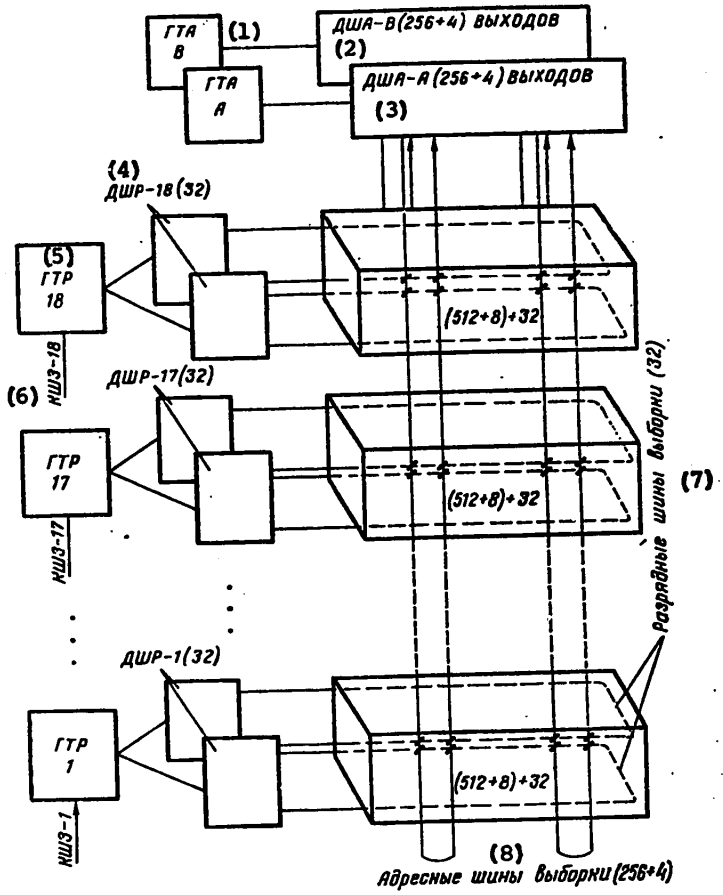

Figure 6.9. Diagram of Magnetic Unit of YeS-1020 Computer

Key:
1. Address current generator
2. Address decoder-B (256 + 4) outputs
3. Address decoder-A (256 + 4) outputs
4. Digit decoder
5. Digit current generator
6. Code write bus
7. Digit selection buses
8. Address selection buses

A total of 512 coordinate buses on each side of the magnetic unit link the ferrite fields of all digits in series and, being connected in pairs, form 256 address selection buses. Each address selection bus penetrates each digit of 64 cores, in each semimatrix of 32 cores with direct branch and 32 cores with reverse branch.

The address selection buses of each of sides A and B of the magnetic unit are connected to the address decoders DShA-A and DShA-B having 256 outputs each.

The digit selection buses of each digit are connected to their own digit decoders (on 32 outputs each). The shaping of write currents in the decoders is controlled by the information being fed through the corresponding code write buses (KShZ). The address (GTA) and digit (GTR) current generators excite the address and digit decoders, respectively.

The selection semicurrent in any address bus acts in each digit on two cores connected by the same digit bus (cores F_1 and F_2 of the first digit). Depending on the direction of the semicurrents, the semicurrents in the digit selection bus coincide either in F_1 in the direction of the first digit current or in F_2 in the direction of the second digit current. Thus, the number of outputs of the address decoder is reduced by half on each side (256 instead of 512 are used) by changing the direction of the digit selection semicurrents.

Besides the 256 address selection buses of the internal storage, there are four additional address buses on each side of the magnetic unit that permit the required capacity of the local (LP) and multiplex (MP) memory to be achieved. Each address bus permits a capacity of 64 two-byte words, i.e., 128 bytes. Thus, the two additional buses (one each on each side) provide a capacity of 256 bytes of local memory while the remaining six additional buses (three each on each side) provide a capacity of 768 bytes of the multiplex memory.

As noted above, the RMN address register contains 18 information digits. The local memory address is located in digits 0-7 and the multiplex memory address is located in digits 0-10.

The internal storage is constructed by the 2.5D type in older models of the Unified Computer System, the same as in the YeS-1020 model, but differs in structural parts and main engineering and operating characteristics (see Table 6.1).

The capacity of a single internal storage unit is equal to 32K 36-digit words in the YeS-1030 model, i.e., it comprises 128 Kbytes. The cycle time is equal to 1.25 microseconds. The main complex of the internal storage contains two units with total capacity of 256 Kbytes. The internal storage in the YeS-1050 model has a capacity from 256 to 1,024 Kbytes arranged in units of 256 Kbytes each. One unit comprises an individual device having total cycle time of 1.25 microseconds. A word 8 bytes long can be selected simultaneously from a single memory unit.

6.4. High-Speed Memory (SOZU)

As is known, modern computer systems have a hierarchical memory structure. The high-speed memory (SOZU) is at one of the first levels. A high-speed memory is

used to increase the productivity of modern data processing systems during exchanges between the internal storage and the arithmetic-logic unit or processor since the basic factor that limits the information processing speed is the speed of data exchange in the internal storage. However, the frequency of access to the cells of the internal storage is usually very irregular. An SOZU with arbitrary access, connected directly to a processor, permits the access time to those cells of the internal storage in which the most frequently used data are stored (for example, intermediate results of calculations, instructions that form the cyclic sections of a program, some service words and so on) to be reduced.

A high-speed memory usually contains information used at the present moment or data which may be required in the very near future. If the required data is not in the SOZU upon access to it, rewriting of the required data unit from the internal storage is organized.

The use of a high-speed memory is feasible according to the following concepts [16]:

1. High-speed memories are used with specific ratio of access time to the main internal storage and speed of the arithmetic-logic device.

2. The high-speed memory in multiprocessor data processing systems reduces the time losses related to switching the processors to the main internal storage.

3. The high-speed memory in microprogram information processing systems can be used to store different user microprograms.

4. The use of a high-speed memory in systems with multilevel microprogramming leads to a significant increase of productivity.

As already mentioned, the basic designation of the high-speed memory is to increase the speed of the central processor. It is natural that the speed of fulfilling programs will be higher, the fewer accesses are made to the main internal storage. Therefore, information exchange between the high-speed memory and the main internal storage may be regarded as optimum if it minimizes the total number of accesses to the internal storage during fulfillment of programs.

Data is exchanged between the main internal storage and the high-speed memory usually by the hardware method. The characteristic feature of the exchange is that both types of memory are connected to each other and moreover each of these devices is connected directly to the central processor.

If the information required by the program to be fulfilled by the central processor is absent in the high-speed memory, the processor either gains access to it to the main internal storage or it is immediately transferred from the main internal storage to the high-speed memory. The exchange is accomplished without interruption of the current program and without interference in the operating system since otherwise the operation of the central processor would be slowed down.

If the information to which the program gains access is not only absent in the high-speed memory but is absent in the main internal storage as well, fulfillment of the current program is interrupted.

The structure of the high-speed memory depends to a considerable degree on the adopted method of information retrieval. The high-speed memory is divided by this feature into one with direct addressing, stack addressing and with associative addressing.

The addresses of the high-speed memory are indicated in explicit form in one with direct addressing in program instructions. An example of this structure of a high-speed memory is that of the common registers in models of the Unified Computer System. Special four-digit addresses related to the high-speed memory are provided in the instructions of the Unified Computer System. The instruction format determines beforehand which addresses are related to the main internal storage and which to the high-speed memory and the program contains complete instructions on which data and for which addresses they are contained in the high-speed memory.

Direct addressing of the high-speed memory will be considered in more detail below on examples of specific models of the Unified Computer System.

The idea of stack structure of the high-speed memory is used in zero-address computers in which there are no instructions in the generally accepted meaning. Each operand occupies a quite specific position in the memory; therefore, there is no need to indicate its address in the instruction. Information exchange between the internal storage and high-speed memory is controlled by special instructions that contain the address of the internal storage cell and the feature which indicates the direction of data transmission: internal storage-high-speed memory, internal storage-processor, processor-internal storage and so on.

The programs of problems solved in zero-address computers consist of an ordered sequence of operational and address syllables of identical digit capacity. The type of syllable is determined by the feature digit. If an address syllable is found in a program, the number is read from the main internal storage by a given address and it is referred to the stack. If an operation code syllable is found in the program, one or two numbers (depending on the type of operation) is selected from the stack, the operation is fulfilled and the result is recorded in the stack.

The symbols representing an address or operation code in a program can follow each other or can be arranged in arbitrary order.

The working principle of a high-speed stack memory is an ordinary storage device connected to a reverse counter, from which the access addresses are fed to the high-speed memory.

The address of the first operand red from the high-speed memory is determined by the initial status of the counter, usually taken as equal to zero.

Each time the next number is read from the stack, a one is subtracted from the contents of the counter, after which the required number is read from the high-speed memory by the address indicated by the counter. This means that a sequential word file can be read from a stack type high-speed memory only from a group of cells with sequentially decreasing numbers. The next new word in the high-speed memory is written by the address indicated by the counter and in this case the contents of the counter are increased by one.

The use of a high-speed stack memory permits practically complete exclusion of transmission of intermediate results between the main internal storage and the central processor. However, this system is inconvenient when organizing operation in real-time and time-sharing modes related to the need for interruption, i.e., disruption of the sequential fulfillment of a single program. Moreover, stack organization of a high-speed memory makes it difficult to use the cells of the stack memory as index registers, cycle counters and registers for storage of return addresses after fulfillment of subroutines.

The associative structure of the high-speed memory is used when organizing exchange on demand between the high-speed memory and the main internal storage. When designing the high-speed memory, the information of each cell of the memory can replace the information of any cell of the main internal storage during fulfillment of the program. Each cell of the high-speed memory contains the information field and address field. The address which this cell would have had if it belonged to the internal storage is written in the address field. When an address is formed in the processor for the next access to the memory, this address is compared primarily to the contents of the address fields of all the cells of the high-speed memory. If conformity is found in any cell, access is gained to this cell and in the opposite case, i.e., if there is no conformity in all the cells of the high-speed memory, access to the main internal storage is gained.

The information field in each cell of the high-speed memory is used to write and store the code contained in the cell of the main internal storage being replaced. The structure of the high-speed memory is called associative because information is retrieved by the conformity of the features, namely of the required address of the cell of the internal storage and the contents of the address fields of the high-speed memory cells, rather than directly by the address of the high-speed memory cell.

The advantage of a high-speed associative memory is the programming simplicity, but its use is now restricted by the complexity of engineering realization.

The high-speed memory in models of the Unified Computer System is frequently called local.

Direct-addressing registers are used as the local memory in the YeS-1020. The local memory is contained in the internal storage of the processor (see 6.2).

The following are located in the local memory: 16 general-purpose registers, 4 registers for floating-point operations, a current program status word, range of channels, working memory of a processor and so on.

The local memory of the YeS-1022, like that in the YeS-1020, is used as common registers and operand registers with floating point to store the information required during operation of selector and multiplex channels. The local memory of the YeS-1022 is an independent high-speed memory constructed on semiconductor flip-flop storage elements in the integrated circuit version with arbitrary selection. The capacity of the local memory is equal to 512 bytes. The access time to the memory is 0.275-0.3 microseconds.

The local memory of the YeS-1030 with random address access has a capacity of 64 words of 36 bits each in each address and is constructed on thin cylindrical magnetic films. The storage element is the surface of a wire coated with a thin film of a ferromagnet. The word winding (read winding) encompasses a wire, while the wire itself (of beryllium bronze) is a write bus and an output winding simultaneously. The minimum access time of the local memory of the YeS-1030 is 0.6 microsecond.

The local memory of the YeS-1050 is made in the form of registers based on integrated circuits with random access. The capacity of the local memory is 96 bytes and access time is 0.24 microsecond.

Chapter 9. Multiprocessor and Multimachine Computer Systems

9.1. General Data on Multiprocessor and Multimachine Computer Systems

The main trend in development of computer equipment is further expansion of the spheres of application of computers and as a consequence conversion from single machines of traditional structure (processor-memory-control-peripheral devices) to computer systems and complexes of diverse configurations with wide range of capabilities.

Solution of such problems as development of large information complexes, operating in the collective-use mode, design of large control systems consisting of a number of facilities and operating in real time and processing large information files places practically unlimited requirements on computer equipment and mainly on speed and storage capacity. However, the speed of a single-processor computer reaches an order of 60 million operations per second [6], i.e., close to the physical limit, at the modern level of development of semiconductor integrated circuit technology. Therefore, a further increase of the speed of computer equipment is possible only by new structural solutions qualitatively different from traditional solutions.

One of the methods of providing more effective joint operation of devices contained in computers is multiprogramming. The multiprogramming principle of operation required a significant change in the structure of second-generation computers. Development of multiprogramming not only permitted an increase of the real productivity of computers, but also made it possible to lay the groundwork for the appearance of machines oriented toward operating in the time-sharing mode.

Flow sheet-program devices that ensure reliability of multiprogram operation, for example, program interrupt and priority flow sheet, memory protection flow sheet, relative addressing flow sheet, CONTROLLER program permanently in the computer memory and so on, were included in the computer structure.

A further desire to increase the productivity of computers led to the development of machines that included several devices that perform the same function (for example, data storage, fulfillment of arithmetic operations and so on). In other words, duplication of different devices (central processors, storage devices, input-output processors and so on) appeared in the computer structure.

Duplication of individual units of the computer and also the presence of special control programs that permit parallel fulfillment of separate operations of the computer process in different devices significantly increase the productivity of the computer due to maximum loading of devices and the reliability of the computer system is enhanced in this case.

A computer system may include different devices with identical functions (for example, those that perform arithmetic operations), autonomous devices of the same type (several parallel models of internal storage) or a hierarchical complex of devices (one central and several auxiliary processors).

A system which contains two or several information processing devices, i.e., processors functioning under unified control, is usually called a multiprocessor system. Parallel operation of several processors that simultaneously fulfill several programs or different parts of a single large program are realized in multiprocessor systems.

Along with multiprocessor computer systems, multimachine computer systems (complexes) are used.

Computer systems containing two or several identical or different independent machines connected to each other through an exchange device are called multimachine computer systems.

Both multiprocessor and multimachine computer complexes are combined into a broader class--computer systems having general features. Multiprocessor and multimachine computer systems are now being developed on the basis of highly productive computers and are the basis for a network of collective-use computer centers.

Computer systems permit on the one hand a considerable increase of computer equipment productivity by parallel operation of devices (for example, of a processor in a multiprocessor system) or of several computers contained in a multimachine complex, and on the other hand they considerably facilitate man-machine interaction, providing a broad capability for direct human interference in the program fulfillment process.

The main requirement on computers used in computer centers is to provide the capability of their operating in the collective-use mode, high reliability, the capability of increasing computing capacity, adpatability to changes in facility control functions and so on.

Computer systems, to meet these requirements, should:

have a developed operating system that ensures simultaneous fulfillment of different programs and that provides access to standard subroutines by users;

have translators from algorithmic languages to facilitate the programmer's work in program preparation;

contain devices that ensure dynamic distribution of memory among programs and also free movement of programs during calculations;

have memory and program protection devices from interference of other programs;

have a time sensor (timer) that permits allocation of the required time to them according to the users' inquiries for work, during which the system is switched automatically to fulfill other programs;

have both hardware and software to organize priorities for simultaneously waiting programs.

One of the basic features of computer systems is the extremely large diversity of their structures. Their classification becomes necessary in this regard. Let us consider the different approaches to classification of computer systems.

According to the principles established during design of computer systems and according to the main fields of application, computer systems are divided into three groups:

1. Computer networks which are developed on the basis of existing computer models by combining territorially dispersed computer centers by means of data transmission apparatus and communications channels. An example of the given group may be the State Computer Center Network (GSVTs). Computer systems used in computer networks are considered in detail in the third section of this textbook.

2. Computing media which are computer systems consisting of a large number of interconnected components, each of which can be program adjusted for information processing, storage and transmission. The use of microprocessors as one of the design elements of computer systems and also the development of miniature high-speed and high-capacity memories are of great interest. All the components in computer media operate in parallel and can simultaneously realize a number of calculating processes. The productivity of computing media may increase essentially without limit with a sufficient number of components without a significant increase of the cost of calculations, i.e., the use of computing media may result in a large saving. However, computing media have not yet found sufficiently broad application.

3. Multiprocessor and multimachine computer systems (complexes) combine the two basic trends in development of computer technology--an increase of reliability and capability of reconfiguration (flexibility). This is achieved due to the modular nature of design. Let us consider the characteristic features of designing this group of computer systems.

Multiprocessor and multimachine computer systems (or complexes) can be classified by different features: designation, type of equipment, method of controlling individual components of the system, permanence of structure, degree of territorial dispersion and so on.

The suggested classification of multiprocessor and multimachine computer systems is presented in Figure 9.1.

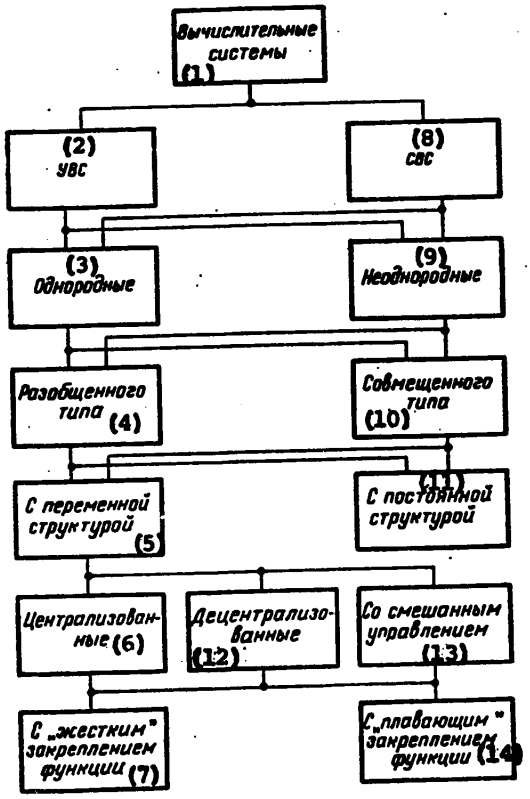

Figure 9.1. Classification of Computer Systems

Key:
1. Computer systems
2. Universal computer system
3. Homogeneous
4. Dispersed type
5. With variable structure
6. Centralized
7. With "rigid" securing of functions
8. Specialized computer system
9. Inhomogeneous
10. Combined type
11. With permanent structure
12. Decentralized
13. With mixed control
14. With "floating" securing of function

Computer systems can be universal (UVS) and specialized (SVS) by designation. Universal computer systems are designed to solve a wide range of problems. Specialized computer systems are oriented toward solution of one or several problems of the same type. The range of problems designed for solution by specialized computer systems usually envisions hardware and software designed specially for this system. Thus, for example, specialized computer systems that control production processes should contain analog-digital converters and vice versa. Devices for displaying the results of information processing specially developed for them,

for example, illuminated display boards in operational control of production, graph plotters and so on, are used extensively in specialized computer systems.

Computer systems are divided into homogeneous and inhomogeneous by type of equipment. Homogeneous systems contain several processors of the same type (internal storage modules and so on) or consist of several program-compatible machines. Inhomogeneous computer systems usually include devices of different type or different computers.

The use of homogeneous computer systems is especially effective in large hierarchical complexes. The presence of equipment of the same type at all control levels permits the use of a unified language and unified software, while the modular principle of design considerably simplifies maintenance and redesign of the system to increase its capacity. It is more convenient to distribute the work between users in homogeneous systems.

The disadvantages of homogeneous systems include incomplete utilization of the productivity of all computers (processors) contained in the system. The efficiency of using them depends on the degree of loading of individual computers (processors).

Inhomogeneous computer systems can be used to increase the utilization efficiency of computers with different productivity. For example, a more productive computer processes information while a less productive computer is used to enter and retrieve information (based on the BESM-6 and MIR).

Special translators and equipment that ensure integration of the devices or individual computers contained in the system are required for normal operation of inhomogeneous systems.

Computer networks can be divided into two types--combined and dispersed--according to the degree of territorial dispersion.

Combined systems include those in which the information transmission time from one computer (processor) to another (another processor) is negligible compared to the time required to process it on one of the machines. Information is transmitted over communications lines from one device (computer) to another usually in parallel code. Multiprocessor systems are usually of the combined type.

The information transmission time over communications channels between computers in dispersed systems is comparable to the problem-solving time on one of the machines and therefore it should be taken into account when investigating the functioning of the system. Information is usually transmitted in sequential code in this case.

Computer systems are divided by permanence of structure into systems with constant and variable structure. The structure of a computer system is understood as its composition and connection between its components.

Two computers contained in a system are regarded as functionally connected if transmission of functional information (programs, input and intermediate data of

problems being solved) from one machine to another is possible during their operation.

A computer system is called oriented according to functional connections if the functional information can be transmitted in only one direction. A computer system is regarded as non-oriented when information is transmitted in both directions. A computer system can also be partially oriented, i.e., it can include both oriented and non-oriented subsystems simultaneously.

Computers contained in a system can be connected by the control principle: control information is fed through one computer (control computer) to another (controlled). The system is called directional if the control communications are constantly directed in one direction. The control communications can be directed in both directions in a nondirectional system.

Both combined and separate communications channels can be used to transmit functional and control information.

A system in which the composition of functional and control communications does not change during functioning is called a computer system with permanent structure. Adaptive systems, i.e., systems in which the structure changes on the basis of analyzing current information, have variable structure. These systems permit one to achieve an optimum state under any variable functioning conditions.

A computer network can be divided into centralized, decentralized and mixed control according to the degree of control centralization.

A typical feature of a centralized system is the presence of a central control computer (processor), called a director-computer. A director-computer controls the functions and exchanges information in a system and coordinates the operation of all machines of the system. Moreover, it can be used for calculations.

The advantage of a centralized system is that optimum methods of problem-solving can be found during its functioning. When solving complex problems, the director-machine distributes the work among individual computers (processors), thus providing a reduction of the total time required for calculations.

Each computer (processor) in a decentralized system operates autonomously and all machines solve their own parts of problems. A decentralized system can have a commutating device through which information is exchanged in the system.

Both centralized and decentralized control principles are realized in systems with mixed control. The entire computer complex in these systems is divided into groups of interacting computer modules with centralized control within each group.

The considered classification does not claim to be complete and can be supplemented with a number of other classification features (for example, in time mode, operating principle of the computer and so on).

The following main indicators--productivity, economy and reliability--can be used to characterize and analyze computer systems.

9.2. Design Principles of Multimachine Computer Systems (Complexes)

During the initial phase of their development, multimachine computer complexes (MMVK) were used to verify the correctness of equipment operation and also to increase the reliability of the results obtained.

Two identical machines simultaneously performed the same task with the same data. Intermediate and final results were compared to each other. Moreover, so-called duplex computer systems were used which consisted of two individual sets of computer equipment, each of which could take on itself the functions of the system and in this case the second set could act as a standby. Thus, one of the computers operated as an active unit and the other was a standby unit. The machines could interchange roles automatically or semi-automatically during operation. Processing was not duplicated in these systems.

Part of the data required to continue calculations could be transmitted periodically from an active computer to the standby computer through a buffer storage (for example, magnetic drum storage connected to both machines). Thus, the main data were stored in duplicate tables of the standby computer during problem-solving. This provided the capability at any moment of time of transferring the active role to the standby computer, which could continue the calculating process of this same task.

Multimachine computer complexes can be divided by this type of organization into two groups: unconnected and connected computer systems.

Unconnected multimachine computer complexes were developed to relieve the central processor of performing data input-output operations externally.

They consist of central and peripheral computers between which there is no direct physical connection (Figure 9.2). There is no jointly used hardware in unconnected multimachine computer complexes. The feasibility of using them is determined by the fact that input-output and calculation operations are combined in time. A small and inexpensive machine performs slow information input-output operations (reading from punch cards, printout and so on), while a central computer performs high-speed operations, exchanging data with external storage devices during calculations.

Practical implementation of these operations can be shown in the following example. Information is transferred from punch cards to magnetic tape, where the assignment pack is formed. A peripheral machine controls these operations. The magnetic tape store is connected to a central computer in which calculating operations are performed. The magnetic tape store servicing a single machine is switched to service another machine by a special automatic switch. Data output is controlled by a peripheral computer to which the magnetic tape store is connected during this time.

The multimachine computer complex has high productivity in this case due to the more efficient use of the central computer. But the total information processing time, including information printout, is increased for each user with this mode

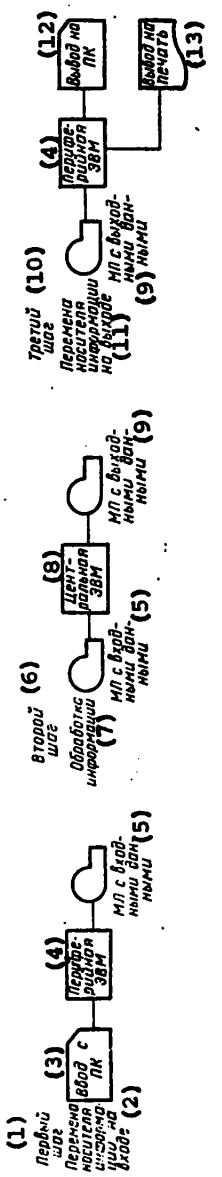

Figure 9.2. Unconnected Computer System with Autonomous Peripheral Computers

Key:
1. First step
2. Change of information carrier at input
3. Input from peripheral complex
4. Peripheral computer
5. Magnetic tape with input data
6. Second step
7. Infomation processing
8. Central computer
9. Magnetic tape with output data
10. Third step
11. Change of information carrier at output
12. Output to peripheral complex
13. Printout

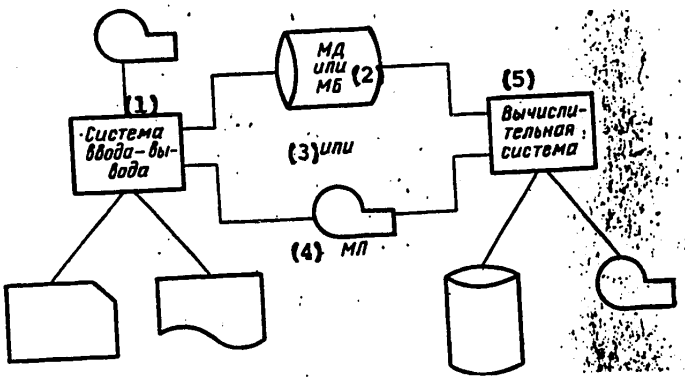

Figure 9.4. Indirectly or Weakly Connected System

Key:
1. Input-output system
2. Magnetic disk or magnetic drum
3. Or
4. Magnetic tape
5. Computer system

of information transmission over input-output channels, the communication of one machine with another through a channel adapter requires matched operation and a specific sequence of actions of all computers. When one machine has access to another, a preliminary message must be transmitted to it through an adapter. The adapter performs the role of control device. It receives the instructions from the communications channel and decodes them, providing connection of the channels and synchronization of operations performed by both channels according to these instructions. Both machines should set the corresponding information read and write programs to working status due to the action of inquiry instructions and the adapter primarily authorizes data transmission.

Multimachine computer complexes began to be developed both abroad and in the USSR on the basis of first-generation computers.

The first multimachine computer complex that became known (the Sage antiaircraft defense sytem, United States, 1955) was a system consisting of 15 computer centers connected by communications lines, in each of which two computers of the same type were used and one of them was a standby computer. The main task of this complex was to ensure high reliability of the computer system.

Homogeneous type multimachine computer complexes have been developed in our country: the M-222 (based on the Minsk-22 computer), the Astra (based on the Minsk-32 computer), the Minimax (based on the M-6000 computer) and the Summa (based on the Elektronika-100 computer); inhomogeneous multimachine computer complexes have been developed on the basis of the BESM-6, Mir-2, Aist (based on the M-20 and Minsk-22 computers) and other computers.

The M-222 multimachine computer complex is a universal homogeneous computer system with variable structure.

since it must wait for the completion of data conversion procedures at the input and output of the system for the entire pack.

Connected multimachine computer complexes include several machines which jointly utilize common hardware, i.e., electric integration between processors is possible in these systems.

Both machines in a connected multimachine computer complex can fulfill two different programs autonomously or in interaction with each other. Interaction between computers remains at the data exchange level since the main computer utilizes the other machine only as an input-output device.

Indirect (weak) or direct contact is possible between computers.

Direct-connect multimachine computer complexes have rigid electrical connection between machines at the level of a common high-speed memory or by direct connection of two high-speed channels. These systems include two or more computers, one of which is a highly productive machine and the remaining ones are used for information input-output and preliminary processing of it (Figure 9.3).

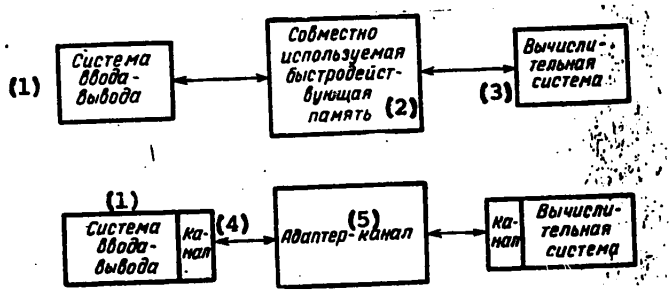

Figure 9.3. Direct-Connected System

Key:
1. Input-output system
2. Jointly used high-speed memory
3. Computer system
4. Channel
5. Adapter channer

In weakly connected systems, the computers have common use of part of the input-output equipment (for example, magnetic disk or magnetic tape external storage). Interaction between the programs being fulfilled in each individual machine is impossible. Exchange is carried out only at the information level. The first computer enters data into a common storage, while the second machine can have access to this storage device at its own initiative or on a signal received from the first computer (Figure 9.4).

Thus, systems with weak connection include such multimachine computer complexes in which the role of work distributor among all the remaining computers engaged in task processing is allocated to a single computer. Computers are usually connected to each other by means of a channel adapter--the channel. Unlike other forms

Productivity can be increased if necessary by simple connection of auxiliary computers. The M-222 multimachine computer complex is a one-dimensional system with two-way communication channels between elementary computers. The number of computers in the system can be varied in the range from 1 to 16. Each computer consists of the Minsk-22 computer and a systems device which includes the operating system unit and communication channel commutator.

The structure of a multimachine computer complex can be changed to isolated subsystems by means of the tuning register available in the system. The communication channel commutator can open or close communications channels depending on the status of the tuning register.

The main features of the M-222 multimachine computer complex consist in the following:

1) homogeneity. All machines are identical. There is no director-computer. Any computer can take on its functions;

2) an n-fold increase of productivity is achieved by simultaneous performance of operations on all n machines of the system;

3) variable structure. The system can be divided by program into subsystems and machines can be noted in the subsystem that jointly perform exchange, conditional and unconditional transfer operations. This method permits one to alter the structure of the system as a function of the task being solved and significantly enhances the structural reliability of the complex;

4) an increase of the system by simple connection;

5) the complex is synchronized by the program method. The operation of all computers of the complex is synchronized by the generator of a single (any) computer of the complex at moments of information exchange.

The Minimax multimachine computer complex is related to those with program-switched communications between individual computers. The complex is constructed on the basis of ASVT (modular computer equipment) hardware and software. Every computer of the multimachine computer complex can have its own individual external devices and moreover can have access to allocated external devices called system devices. This complex can be used in ASU.

The Summa (minicomputer control system) multimachine computer complex is related to homogeneous complexes (it has a programmable structure), has the capability of increasing its capacity over a broad range, is characterized by high reliability and is constructed on the basis of Soviet Elektronika-100 and Elektronika-100I minicomputers. The Summa multimachine computer complex consists of computers of the same type. Two-directional program-switched communications channels are used to exchange control information and data between computers of the multimachine computer complex. The multimachine computer complex includes Elektronika-100 computers and a systems device that permits the structure of the multimachine computer complex to be programmed and that permits systems interactions of the machines.

The systems device is connected to one computer through standard channels for external devices and to the systems devices of four other computers through intermachine communications channels.

Two functional modes are most frequently realized in the Summa multimachine computer complex: one modes is used when solving scientific and technical and information problems and is the collective-use mode and the other is oriented toward real-time servicing of the priority flow of declarations.

Development of multimachine complexes based on models of the Unified Computer System is of special interest. The capability of combining several machines into a Unified Computer System is embodied both in the structure and software of the Unified Computer system.

Communications between individual computers can be accomplished at the level of any of independent, logically independent devices (processors, internal storage, multiplex and selector channels and so on) by means of hardware and software.

Depending on the type of hardware used, the following levels of communications between computers are distinguished:

1. At the channel level by means of the "channel-channel" adapter. The "channel-channel" adapter (the YeS-4060 device) is used to exchange data between input-output channels of the Unified Computer System and transmits information from the internal storage of one computer to another through the channels of these machines. The adapter can join multiplex and selector channels and also two selector channels. It operates only in the monopole mode and transmits data at the speed of the slowly operating channel (of the two connected channels). It performs the functions of external device control, which is selected by the channel, for each of the channels to which the adapter is connected. The adapter answers inquiries of the channel and receives and decodes instructions of the channel. The adapter differs from any other external device control by the fact that it does not control input-output devices but only provides communication between channels and synchronizes their operation.

The "channel-channel" adapter consists of two control units, each of which is connected to an input-output interface, and services its own channel. The control units are connected directly to each other by several signal lines and common single-byte buffer register to which the information transmitted from one channel to another is fed.

2. At the level of external device controls by means of a two-channel switch that permits working, for example, with two channels belonging to different machines.

3. At the level of the external memory or input-output devices by means of a two-way switch. Communication at this level is feasible if high speed is not required. This method provides a considerable increase of the volumes of program and numerical information simultaneously accessible to processors in multiprogram operation. The external device controls communicate with the two channels through a standard input-output interface. The external device control operates with the channel which first sent the inquiry to work with an external storage device.

4. At the level of data transmission equipment by means of auxiliary remote communications control devices.

5. At the level of a common internal storage by means of the console that switches the memory units. This communication permits one to organize control of the calculating process of a unified operating system and to achieve simultaneous solution of independent parts of the same problem. Parallel access of the processors to the memory units is authorized due to the double communications interface of the memory units with the processors and priority circuit. The reconfiguration console connected to the system permits one or several memory units to be excluded and also permits distribution of the memory units among processors.

6. At the processor level by means of direct control devices. In this case signals of external interruptions and control information is transmitted between processors to synchronize the unified calculating process.

Multimachine computer systems based on older models of the Unified Computer System, for example, the YeS-1050 can be constructed by using any communications level, but the functional efficiency of the computer complex will be different. Younger models of the Unified computer complex can be connected only at the channel or common external device level.

The main task of organizing communications between machines at any level, as is known, includes the capability of using common information files and programs by connected processors of the system. The most flexible and highest speed is communication of processors through a common internal storage field. In this case the calculating capability of the system and the utilization efficiency of the internal storage are increased sharply. Moreover, the calculating system can control a unified operating system.

Based on models of the Unified Computer System, calculating complexes of two machines are primarily developed. A diagram of a two-processor computer system that includes different types of communications is presented in Figure 9.5. Specifically, the VK-1010 multimachine computer complex has been organized on the basis of two YeS-1030 computers connected by direct control buses to the computer complex status unit (BSVK).

The VK-1010 computer complex can operate in five different modes:

1. The computer complex is in working order and operates in the "hot" standby mode. In this case one of the machines is the main one and the other is a reserve. Both the main and reserve machines receive information coming from external devices and process it by the same algorithm, but the information is sent to external devices only by the main computer. If the main computer is unable to transmit the information for any reason, the reserve computer takes on the functions of the main one, leaving the main computer as the reserve. The YeS-1030 computers are switched to the MAIN and RESERVE modes either by program or by an operator from a dispatcher's control console.

2. One of the machines is in working order and solves problems without duplication and the second computer is also in working order but is in the preventive

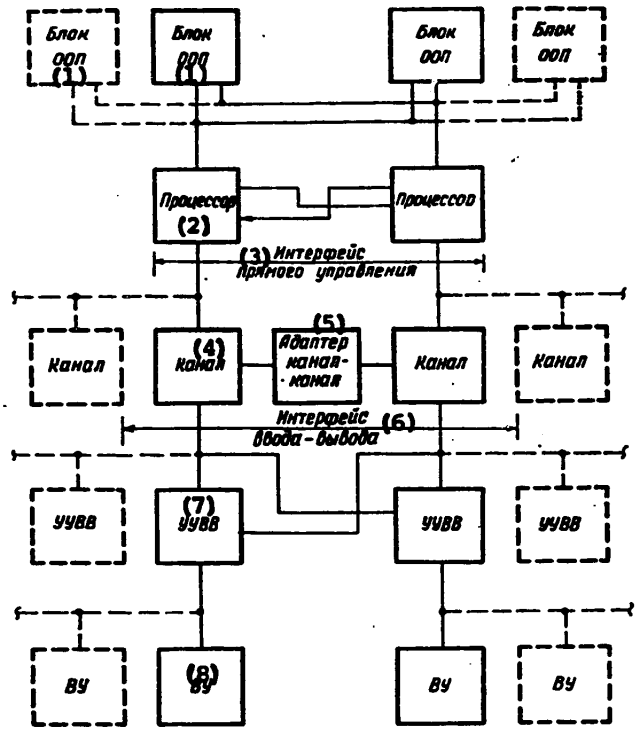

Figure 9.5. Diagram of Two-Processor Computer System

Key:
1. Main internal storage unit
2. Processor
3. Direct control interface
4. Channel
5. Channel-channel adapter
6. Input-output interface
7. Input-output control device
8. External device

maintenance mode during this time. If the main machine malfunctions, the preventive maintenance work on the second machine can be stopped and it can be switched to solve the basic program. The moment that the main computer is switched off can not be predicted beforehand since it is determined by the resulting situation.

3. One of the machines is inoperable. The problem is solved on the functioning computer while the inoperable computer is checked by maintenance tests. If a malfunction is detected, the computer is switched to the repair mode by the operator from the computer complex control console. If a malfunction is not detected, then a breakdown in the computer is recorded and the machine continues in the preventive maintenance state.

4. One of the machines is in repair. After completion of repairs the computer is transferred to the preventive maintenance mode to determine the quality of repair.

5. The autonomous mode of operation of machines contained in the complex. Each computer operates with its own set of external devices independently of the other.

The states of computers considered above are shown in Table 9.1.

Table 9.1.

YeS-1030(1)	YeS-1030(2)
ON, Functioning, Main	ON, Functioning, Reserve
Functioning, Main	Functioning, Preventive Maintenance
Functioning, Main	Malfunctioning, Preventive Maintenance
Functioning, Main	Malfunctioning, In Repair
Functioning, Independent	Functioning, Independent

The operating mode of the computer complex can be assigned by program or by direct control instructions or (depending on the developed situation) from the complex control console.

The VK-1010 computer complex provides:

organization of a common internal storage field, i.e., independent access on the part of each of two processors through two mainline systems and the capability of simultaneous access of each of the processors to different internal storage units through a common internal storage unit;

exchange of control signals of computer status for automatic switching of the operating modes of the computers;

exchange of control information between the processors of two YeS-1030 computers of the complex through direct control channels;

exchange of information between two machines by means of the "channel-channel" adapter;

connection of external storage devices to any of two machines.

A complex of two YeS-1030 machines using minicomputers as buffer processors has considerably greater capabilities. Minicomputers take on themselves the functions of the low distribution of users and are communication processors.

Creation of a two-processor system with common internal storage field is possible on the basis of YeS-1030 and YeS-1050 models or of two YeS-1050 machines. The system includes a reconfiguration console to assign the operating models of the complex, physical distribution of system resources (internal storage, external device controls and the external devices themselves) between processors and to exclude malfunctioning devices from the system.

A two-processor system has direct control devices that include auxiliary lines which are used in specific operating modes to synchronize the work of processors and to transmit control information.

The processors of a two-processor system can operate in three modes: MULTISYSTEM, MODEL and SPLIT SYSTEM.

In the MULTISYSTEM mode, two processors are combined into a unified system with internal and external storage split between them and also with input-output devices to control the common multiprocessor control program.

Independent operation of the computer organized by a single-processor control program is accomplished in the MODEL mode. Multisystem devices are not used and multisystem signals are not emitted and are not received.

In the SPLIT SYSTEM mode, the multiprocessor control program is carried out by using a single processor, but it has access to any of two processors. This mode can be used if one of the processors malfunctions. The action of direct control instructions is blocked in this case with communication at the processor level. Multisystem instructions are not issued and are not received since the processors operate independently. Conversion from the MODEL to the SPLIT SYSTEM mode is made from the system reconfiguration console.

Work in the modes described above is organized by means of a developed operating system that includes a control program which ensures multiprogramming with variable number of tasks.

The characteristic feature of the operating system is the use of processors as a unified resource when processing the assignment priority, performing input-output operations for the task solved by a single processor using another and processing error signals in an apparatus by using two processors.

The required devices to organize a time-sharing mode are provided in older models of YeS computers (for example, the YeS-1050) in which a service period by the processor is made available to each independent task sequentially (in the order of priority and sequence) with subsequent return to the wait sequence and repetition of the servicing procedure.

9.3. Design Principles of Multiprocessor Computer Systems (Complexes)

Special attention is now being devoted to development of multiprocessor computer complexes (MPVK) and in this case the processors of these systems have equal capabilities and they are MPVK assemblies. Communication between them is accomplished on the basis of standard interfaces.

The main role in development of multiprocessor computer complexes is to increase the productivity of systems by providing the capability of parallel fulfillment of independent tasks, inc asing the operating efficiency and improving the low distribution in the system, providing more economical servicing of outside assignments and those with peak loads and achieving a high effective utilization factor of resources to develop new types of configuration of the complex.

The advantages of multiprocessor computer complexes compared to multimachine computer complexes in speed are determined by the following factors:

1. Solution of fundamental problem-oriented tasks such as automation of large facility design, working out different versions of current and future plans for development of the country's economy and so, reduces to carrying out a large number of calculating processes that utilize common data. The same systems programs (operating system, programming automation system), applied program packs and common data for tasks being solved simultaneously can be used for solving these problems. All these data should be stored in the memory of each computer in a multimachine complex and there is no need to duplicate these data in the memory in a multiprocessor computer system.

2. Auxiliary devices for synchronizing these computers are required in a multimachine complex, each computer of which controls its own operating system, when solving several problems with common data.

3. The efficiency of utilizing the capacity of the internal and external storage used by separate problems is considerably enhanced in multiprocessor complexes. Most problems require small memory capacities during most time intervals and this capacity increases only during temporary peak time segments. Memory capacity is selected according to peak situations in single-processor system so as not to reduce the overall speed of problem-solving due to restrictions of the memory.

Simultaneous solution on different processors is possible in multiprocessor computer complexes when solving problems with small memory capacities. If a sharp increase of memory capacity is required during each time interval, the entire memory is set at the disposal of a single problem. The main features of MPVK design include the following:

the system includes one or several processors;

the central memory of the MPVK should be in common usage and access to it from other processors of the system should be provided;

the MPVK should have common access to all the input-output devices, including channels;

the MPVK should have a unified operating system that controls all hardware and software;

interaction of the hardware and software components at all levels should be provided in MPVK: at the systems software level, at the program level when solving user problems (the capability of task redistribution), at the data exchange level, hardware interruption level and so on.

The latter feature of MPVK significantly distinguishes it from multimachine computer complexes, in which communication can be established only at the information level.

Methods of connecting diffe. nt functional units of the system to each other is of the most important significance for organization of a multiprocessor computer

complex since the efficiency of the MPVK is determined largely by the degree of parallellism or time combination of the operation of all devices of the system.

Let us consider some types of organizing multiprocessor computer systems.

1. Systems with Common or Time-Shared Bus

This system is organized so that all functional units are connected to a single common connecting bus, which can have the width of one complete word (byte) or one bit. The less the width of the bus, the more complex is organization of system control. The bus that links modules can be a single two-way (Figure 9.6) or they can be two one-way. Information is transmitted between modules through the bus in the time-sharing mode. The memory is accessible to all the units of the system with this organization.

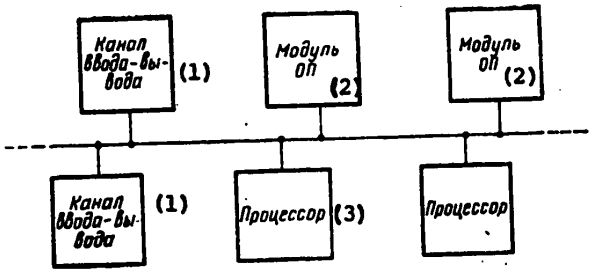

Figure 9.6. Organization of System with Common or Time-Shared Bus

Key:
1. Input-output channel
2. Internal storage module
3. Processor

Each information pack fed to the bus should contain, besides the data subject to transmission, the address of the unit to which it should be directed. Conflicts among several packs fed to a single unit cannot arise in this system since the bus contains only one pack at each moment of time, while all the remaining information sources should wait until the bus is free, i.e., conflicts in the system are prevented automatically. Each unit connected to the bus should have equipment that recognizes the address in the pack.

A system with a time-shared bus is very flexible and permits easy alteration of the number of functional units. Moreover, the system has low cost, low productivity which is limited by the speed of the data transmission line and low simultaneous utilization efficiency of all available units. An MPVK with common or time-shared bus is usually employed in low-power complexes.

2. Cross-Switching Systems

A cross-switching MPVK is presented in Figure 9.7. This complex permits connection of any memory module to any processor or to any input-output device. Unlike

switching with time-shared bus, this method of switching is called the space-sharing method. Physical contact for the entire period of information transmission is established between any two units and the information transmission speed increases in this case. Moreover, several transmission paths can be established simultaneously.

The switching matrix is completely separated from the functional units of the system and can be designed by the modular principle, which permits rather simple expansion of it if the switching matrix has adequate capacity. But the switching matrix is in itself very complicated. Thus, for example, a matrix for eight processors and 16 memory modules contains more components than the processor. Conflicts during inquiries of the same memory module are resolved in the switching matrix. A cross-switched system has less flexibility compared to the previous system.

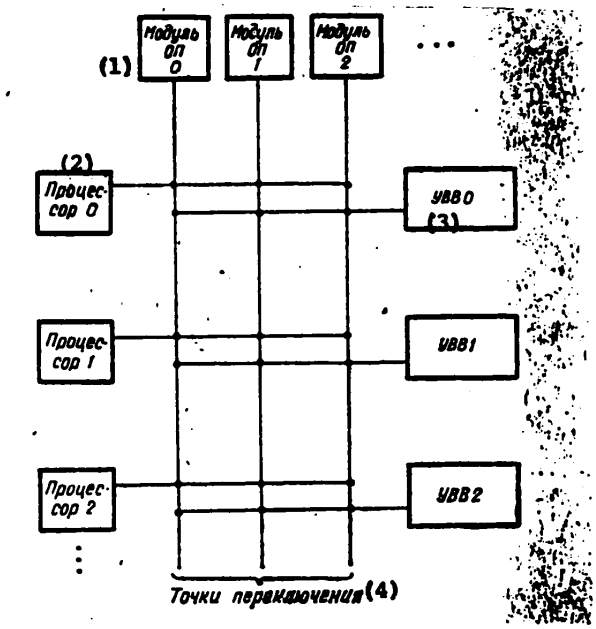

Figure 9.7. Organization of Cross-Switched System

Key:
1. Internal storage module
2. Processor
3. Input-output device
4. Switching points

An MPVK with cross-switching consists of functional units comparatively simple in structure, provides high transmission speed and permits an increase of the system's efficiency by expanding it through increasing the size of the switching matrix. Expanding the system does not require alteration of the software. The main disadvantage of MPVK with cross-switching is its complexity and high cost.

3. Multibus-Multi-input Systems

Multibus-multi-input computer systems permit information to be transmitted over several lines simultaneously.

The memory modules in this system should have several inputs and should also be equipped with control circuits to resolve conflicts in those cases when two or more processors or input-output devices require access to the same memory module within a single cycle. Each processor and input-output control device in a multiprocessor computer complex of this type is connected to a separate input of the central memory module by means of an individual bus.

The maximum number of modules connected to the memory unit is limited by the number of inputs of the memory module. An input expander or multiplexers can be used to increase the number of inputs and in this case the information transmission speed should not exceed the permissible speed for a single input.

Conflicts frequently occur in systems with multi-input memory, which are resolved by the affiliation principle, i.e., the priority of information transmission with simultaneous access is given to the processor which gains access to "its own" memory module (Figure 9.8).

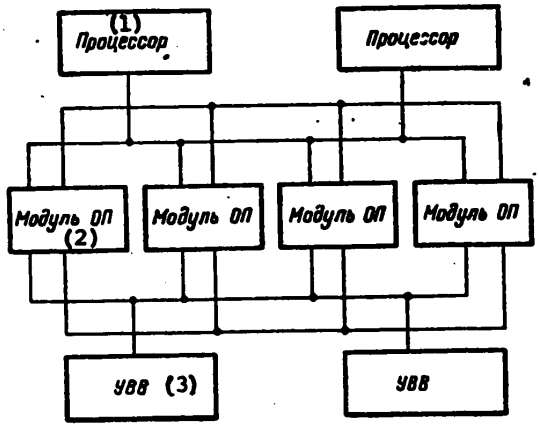

Figure 9.8. Simplified Organizational Diagram of Multibus-Multi-input System

Key:
1. Processor
2. Internal storage module
3. Input-output device

The width of the data transmission line is selected on the basis of convenience and economy. If the main unit of stored information is a word and the width of the data transmission line is smaller than a word, then a special register for expansion and convolution of words and also special control circuits that guarantee the correctness and continuity of transmitted information are required.

All memory units must be connected to each processor of the system since each processor has its own memory unit in which special tables and control information are stored. This method of connecting the modules of the processor to the memory modules reduces the reliability of the system since the capability of receiving information from the memory module belonging to it and of continuing calculations made earlier by a processor that failed is lost with failure of any of the processors.

The memory module in all complexes of similar configuration should recognize and process requests for access to specific memory cells. The control circuits of the memory module should resolve conflicts during simultaneous access.

The great advantage of these systems is that switching apparatus is not required for the processor. The complex can operate in the single-processor configuration mode, consisting of the same functional units without changing their design. The complex has high information transmission speed.

The disadvantages of these systems should include limitation on size and number of possible configurations determined by the limitation of the number and types of available inputs in the memory modules, large number of cables and plugs and also the presence of expensive storage devices.

4. Computer Complexes with Mainline Processing

Increase of information processing speed is achieved in the types of organization of complexes considered above by increasing the number of processors, i.e., by parallel fulfillment of operations. Organization of a computer system with mainline structure includes division of operations (instructions) into several steps and in this case each step is performed by a separate set of equipment.

After the first step of the operation has been completed for the first pair of numbers, the unit that implements this step may begin to fulfill the first step on the second pair of numbers and during this time the first pair of numbers is fed to the second unit, where the second step of the operation is implemented. When the first pair of numbers is fed to the unit implementing the third step of the operation, the second pair of numbers is fed to the second unit while the first unit begins to process the third pair of numbers and so on. An identical time to perform all steps of the operation must be selected with this organization of the complex. This time is assumed equal to the longest step.

The organization described above is suitable for a specific class of problems characterized by repetition of operations of the same time, for example, arithmetic operations on a sequence of operands. Specially developed software and specific hardware are required to implement it that ensure parallel completion of different elementary actions. The mainline method provides the greater effectiveness, the more complicated the operations to be performed are.

The main advantages of multiprocessor computer complexes, due to which they find ever broader application, especially in computer networks, should be noted:

high readiness and reliability;

functional flexibility;

high efficiency and productivity.

The readiness of the complex is usually understood as the degree of capability of the complex to perform its own functions at the moment when it is required for data processing. Readiness time consists of the idle time and operating time of the complex. Therefore, this characteristic is closely related to the operating reliability of the complex.

Recent investigations [22] showed that the reliability of a multiprocessor computer complex is higher than that of a multimachine computer complex. This is related to the capability of access of all processors to the entire memory and the capacity of the multiprocessor computer complex to rapid reconfiguration.

The flexibility of the system is not only the capability of the system to rearrange its own configuration comparatively easily, but also to rearrange the functional properties of the system that ensure high readiness and reliability of the system with minimum composition. This quality of the system permits all systems resources to be used by each user (task) and also provides access of several programs to large data bases.

Efficiency and productivity are determined in multiprocessor systems the same as in single-processor computers. It should be noted that the utilization efficiency of multiprocessor complexes is especially high when solving large problems if a restriction is placed on the time of solving them. Solution of these problems may be impossible in a single-processor computer.

The main disadvantages of multiprocessor computer complexes should include the following:

complexity of system programming;

complexity of checking system programs and large expenditures on organization of checking;

an increase of efficiency with an increase of the number of functional units is hindered by an increase in the cost of the complex;

the capability of changing the configuration of the complex and of increasing the methods of communication is limited by the apparatus properties of functional units, namely the presence of time-sharing of a common bus, the number of inputs to the memory, specifications imposed by the interface and the presence of delays in transmission of signals determined by the length of the cables between units.

The El'brus-1 multiprocessor computer complex having modular structure has been developed in our country. The following capabilities are provided in this multiprocessor computer complex depending on its makeup: an increase of productivity

Table 9.2.

Type of Device	Number of Devices: Single-processor El-brus-1	Number of Devices: 10-Processor El'brus-1
Central processor	1	10
Main storage	2	16
Main storage commutator	1	4
Input-output processor	1	4
Data receive-transmit processor	1	16
Synchronizer	1	1
Central engineering console	1	1
External storage		
Magnetic drum and magnetic disk storage control devices	1	4
Magnetic drum store	2	32
Magnetic disk store	4(8)	32(48)
Magnetic tape storage control devices	2	8
Magnetic tape store	4(12)	32(64)
Input-output devices		
Punch card input	2(4)	8(16)
Punch card output	2	4(16)
Papertape input	2	4(8)
Papertape output	2	2(4)
Alphanumeric printer	2(6)	16(32)
Typewriter	2(4)	4(16)
Complex of four alphanumeric displays (YeS-7906)	1(4)	2(32)
Graphic input-output devices		
Graphic recorder (YeS-7051, 7052, 7053)	(2)	(8)
Graph plotter magnetic reading device (YeS-7050)	(2)	(8)
CRT alphanumeric and graphic information input-output device (YeS-7064)	(1)	(8)
Data preparation device		
Punch card data preparation device (YeS-9011, YeS-9010)	2(8)	16(48)
Papertape data preparation device (YeS-9024)	2	2(8)
Magnetic tape data preparation device (YeS-9001)	2(4)	4(16)

by increasing the number of processes (1-10), an increase of internal storage capacity (0.5-8 million characters and 4-32 modules), an increase of the number of input-output processor modules (1-4), essentially unlimited expansion of the external memory capacity (magnetic drum, magnetic disk and magnetic tape modules) and an increase of the number of data receiving-transmission modules (1-16). Each module has built-in verification. The module is switched off if a malfunction occurs. The given reliability of the complex is provided by redundancy of modules of devices of the same type (KM).

The modular system provides the capability of adapting the computer complex to the class of problems being solved for more efficient utilization of equipment and also permits a gradual increase and development of the complex without disturbing the operation of devices introduced earlier.

A block diagram of the El'brus-1 multiprocessor computer complex is shown in Figure 9.9 and its makeup is presented in Table 9.2.

The productivity of the El-brus-1 single-processor system is 1.5 million operations per second and that of the 10-processor complex is 12 million operations per second. The internal storage capacity is 576 Kbytes and 4,608 Kbytes, respectively.

Nonaddress command structure is adopted in the El'brus-1 computer complex. This structure has great advantages. It provides:

code compactness;

simple and efficient translation of programs from high-level algorithmic languages compared to the Unified Computer System;

dynamic resource distribution;

practically unlimited virtual memory;

distribution of internal memory in segments of variable length;

hardware realization of standard algorithms of the operating system.

The central processor carries out dynamic distribution of high-speed registers, distribution of internal storage in segments of variable length, organization of parallel processes, automatic calculation of index when processing multidimensional files and working with fields of variable length and with numbers of different formats (32, 64 and 128 digits) during data processing.

The operation of addition with fixed point is performed in the processor within 520 nanoseconds and that with floating point is performed within 780 nanoseconds, multiplication of 32-digit numbers with fixed point requires 780 nanoseconds and logic operations and operations with fields are performed within 520 nanoseconds.

The computer complex contains a special processor which can be connected in place of one of 10 processors. Its productivity is three million operations per second.

algorithm. The operating system allocates one or several pages of the mathematical memory (depending on the capacity of the file) for each data bit and the first word of the file described by the descriptor is placed in the first word of the page.

The capacity of one internal storage unit is 4K 36-digit words and access time is 1.2 microseconds. The internal storage is connected to the central processor and input-output processors through the internal storage commutator. Each commutator organizes communication of four internal storage modules with the information user (the maximum number is 14).

A fast channel unit and standard channel unit are used to exchange information between internal storage and external devices. The fast channel unit provides connection of up to 64 magnetic drum and interchangeable magnetic disk stores with simultaneous operation of four of them. There are a total of two fast channels.

The standard channel unit permits connection of 256 external devices (magnetic tape store and input-output devices) to it and 16 devices can operate simultaneously.

The information exchange rate through the fast channel is up to four million bytes per second and that through the standard channel is 1.3 million bytes per second.

The El'brus-1 multiprocessor computer complex is designed on the basis of integrated circuits and is related by its component base to third-generation computers. However, development of the principles imparted in this complex made it possible to work out and begin production of the El'brus-2 multiprocessor computer complex with productivity of more than 100 million operations per second. It is designed on the basis of microcircuits with high degree of integration (large integrated circuits) and is therefore related to fourth-generation computers.

The software designed for the El'brus-1 multiprocessor computer complex can be fully utilized for the El'brus-2 complex as well.

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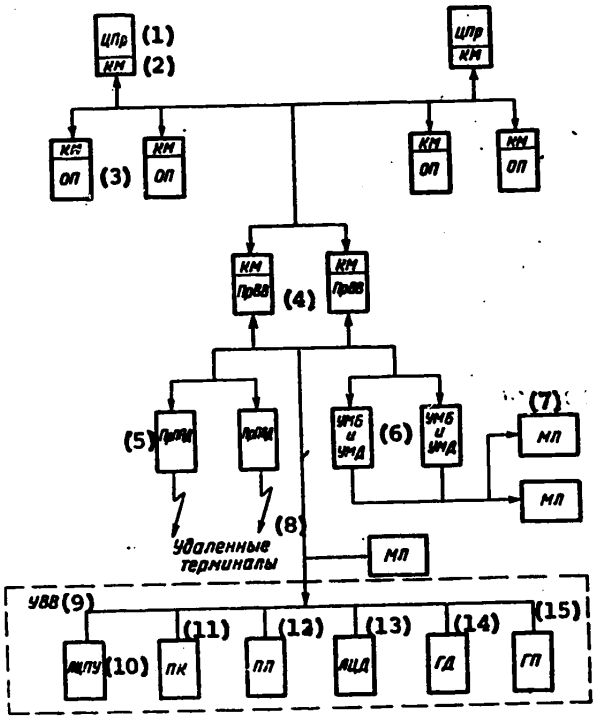

Figure 9.9. Block Diagram of El'brus-1 Multiprocessor Computer Complex

Key:

1. Central processor
2. Commutator
3. Internal storage
4. Input-output processor
5. Data receive-transmit processor
6. Magnetic drum and magnetic disk device
7. Papertape
8. Remote terminals
9. Input-output device
10. Alphanumeric printer
11. Punch card
12. Papertape
13. Alphanumeric display
14. Graphic display
15. Graph plotter

The high-speed memory (SOP) of the complex is distributed by processors and is organized on the functional principle. The high-speed memory consists of five parts: fast virtual registers for storage of the top of the stack, local memory with direct addressing, associative memory for storage of the common data of two processors, associative memory for storage of frequently repeated procedures and buffer memory for apparatus advance pumping of data files.

The internal storage has dynamic distribution and the mathematical pages have a capacity of 512 words each. The information bit of internal storage exchange with the processor has arbitrary length (with discreteness up to a word) and the length is determined by the descriptor that describes this data file on the basis of an

INFORMATION CODING AND DATA PREPARATION

Moscow EVM I VYCHISLITEL'NYYE SETI in Russian 1980 (signed to press 20 May 80) pp 24-45, 72-104, 185-224, 303-314, 319-320

[Excerpts from the book "Computers and Computer Networks" by Vasiliy Nikolayevich Kriushin, Inna Nikolayevna Buravtseva, Nina Mikhaylovna Pushkina and Nina Grigor'yevna Chernyak, Izdatel'stvo "Statistika", 18,000 copies, 328 pages]

[Text] 2.1. Methods of Encoding Economic Information for Machine Processing

2.1.1. Main Data on Machine Conversion of Information

Any data that provides a concept of one or another aspect of the material world and of the processes occurring in it (natural phenomena, events in social life, in technology and so on) is understood as information in the broad meaning of the word.

Information is represented concretely by messages (in the form of speech, text, digital data, images and so on). Thus, a message is information embodied in material form. Messages can be analog and digital.

There are various types of information depending on the object of its use. One of the types of information is economic information which is related to social production, distribution, exchange and consumption of material goods. It reflects phenomena and events occurring in the production and economic activity of enterprises and organizations.

Economic information performs the function of planning, regulation, monitoring, accounting and bookkeeping and has a number of characteristic features such as:

it is discrete since it reflects the activity of a facility through a system of natural and cost indicators represented in alphanumeric form.

it is characterized by a large mass character, comparatively simple mathematical processing and the need for multiple grouping and sampling;

initial information is usually recorded in documents and is subject to rewriting to machine carriers for computer entry.

Economic information on functions during management is divided into planning, accounting, statistical and so on.

Discrete information, including economic information, is convenient by the fact that it can be expressed by a set of elements of finite length.

Let us consider the main concepts and terms of machine display of information. The smallest information unit is the bit (binary digit).

The elements which make up a digital message are called symbols. A symbol is a graphical sign that depicts the number, letter, service, mathematical and other signs. It is frequently called a syllable--a group of binary digits used to represent a symbol--as a machine unit of information. An eight-digit syllable--a byte that has become the basic machine unit of information--is used to represent the symbol in the YeS EVM [Unified computer system]. The set of symbols forms an alphabet. The number of symbols in the alphabet is called the alphabet capacity. The binary alphabet having two symbols zero and one has become widely used in computers. If number and letter values are assigned to information elements, the information is called alphanumeric.

The aggregate of symbols in an alphabet is a word. Word length is determined by the number of symbols contained in it. This is the number of binary digits in the binary system of calculation. A word is usually employed in machines to represent alphanumeric information.

The length of a machine word for a specific type of machine can be either a constant or variable value. For example, word length is a specific value for first- and second-generation computers. The length of the alphanumeric word is a variable value (1-256 bytes) in the unified computer system. A machine word may be a binary word with floating or fixed point, instruction or decimal numbers.

The aggregate of several machine words combined by a unified mean is called a phrase or a recording. A group of phrases (recordings) sequentially arranged on an external memory carrier, recorded from an external memory or read in it by a single instruction, is called a unit. Several units containing recordings combined by some feature into an information file is called a file.

Input data must be transformed to the desired results when solving any problem. This action is called information conversion. In this case the input data and results of calculations are expressed by different words but the recorded data are expressed by the same alphabet. Information can also be converted by translation from one alphabet to another. Thus, for example, using the symbols 0 and 1, one can, as was shown earlier, convert numbers in decimal notation to binary notation (a binary alphabet).

Information conversion in a computer is preceded by transfer of it from machine carriers or from different external devices. The results of calculations may in turn be transferred via input-output channels to external devices. Information is

entered into a computer and is exchanged between the computer and external devices using specific codes.

2.1.2. Information Coding

To display information in a computer, the alphabet symbols of the computer are encoded by a specific set of binary numbers which are arranged in the digit matrix of the machine having a specific number of digits. Thus, coding is conversion of information from one alphabet to another equivalent alphabet by using its symbols.

The byte (syllable) consisting of eight bits (binary digits) is used in the YeS EVM as the basic minimal addressable unit of information. The code of an alphanumeric symbol or two decimal numbers encoded in binary-decimal notation or two 16-digit numbers and any set of eight binary digits can be located in a byte. Eight information bits permit one to arrange 2^8 or 256 different symbols in binary notation (from symbol 00000000 to 11111111) in a byte. Other units of information (halfword, word and double word) are multiples of the basic structural unit--the byte. The byte structure of data will be outlined in Chapter 3.

Devices with various encoding systems that utilize codes of different length are now used for data preparation. Individual systems are used to encode digital and alphanumeric information. the most widespread are systems based on GOSTs [State standard] 10859-64, 13052-74, 19768-74 and 19769-74.

Three types of codes--KOI-7, KOI-8 and DKOI--are mainly used in models of the YeS EVM. However, the presence of preliminary processing units permits information to be recoded from KOI-8 to DKOI and vice versa in the unified computer system.

KOI-7--a seven-bit code for information exchange (GOST 13052-74)--is designed to display alphanumeric information at the inputs and outputs of data transmission equipment over communications lines and also to place information on papertapes.

The table for encoding symbols with seven-digit codes is shown in Figure 2.1.

All the symbols of the alphanumeric codes are subdivided into two classes--graphic and control (special). Graphic symbols include capital and lower case letters, numbers and symbols. Control (special) symbols include mainly communications symbols which serve a control function when establishing communications and for determining the formats of transmitted data. For example, PUS means empty, NZ means beginning of heading, NT means beginning of text, KT means end of text, KP means end of transmission and so on.

The KOI-7 table consists of two parts--the left part is called the first or Latin register and the right part is called the second or Russian register. A seven-bit binary code E_7, E_6, E_5, E_4, E_3, E_2 and E_1 corresponds to each symbol of the table. The code of the symbol is determined by the position found at the intersection of the number of the column and line of the code table. For example, the letter Ye in the Russian register position 14/5) corresponds to binary code 1100101 and in the Latin register (position 4/5) it corresponds to 1000101. The type of alphabet is indicated in front of the information by the symbols LAT or RUS (VKh and VYKh in GOST 13052-74).

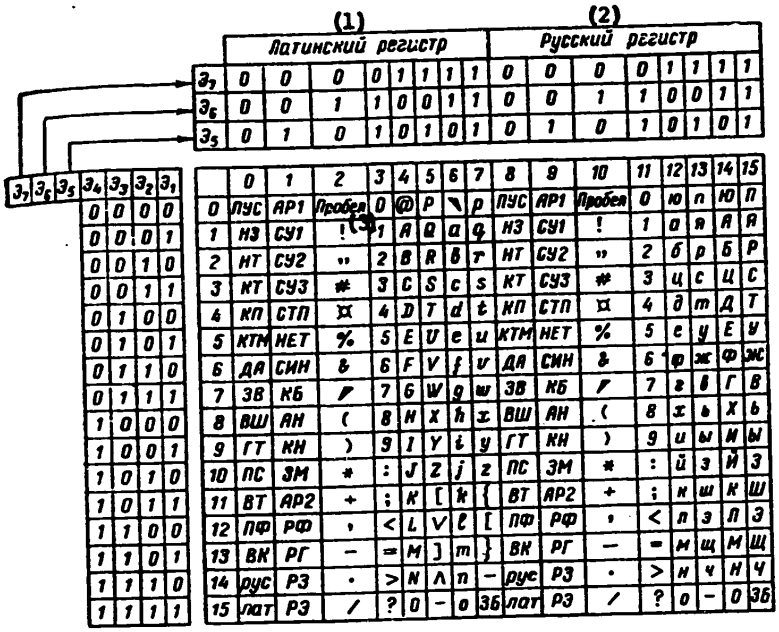

Figure 2.1. Table for Encoding Symbols with Seven-Bit Codes for Information Exchange (KOI-7)

Key:
1. Latin register
2. Russian register
3. Space

A seven-bit code is the basic code for data transmission equipment and input-output devices of user stations, but it is inconvenient for internal processing of information in machines. Because of this, the basic codes for the YeS EVM are KOI-8 (an eight-bit information exchange code) and DKOI (binary information exchange and processing code)--GOST 19768-74. The advantage of these codes is the capability of encoding a large number of symbols (up to 256).

The KOI-8 is designed to exchange alphanumeric information with magnetic carriers (magnetic tapes, disks and cards). It is constructed on the basis of the seven-bit KOI-7 code. The seven smallest bits of an eight-bit code correspond to the values of a seven-bit code. The value of the largest, eighth bit of the KOI-8 determines to which register the code belongs. If the eighth bit contains a zero, this means that the symbol belongs to the first (Latin) register. A value of one accordingly determines the affiliation of the symbol code to the second (Russian) register.

The KOI-8 was developed with adherence to the recommendations of the international ISO [expansion unknown] organization. The list of service and graphic symbols established by this standard provides the capability not only of computer and logic processing of information but also exchange of information over communications lines both within the country and over international communications lines.

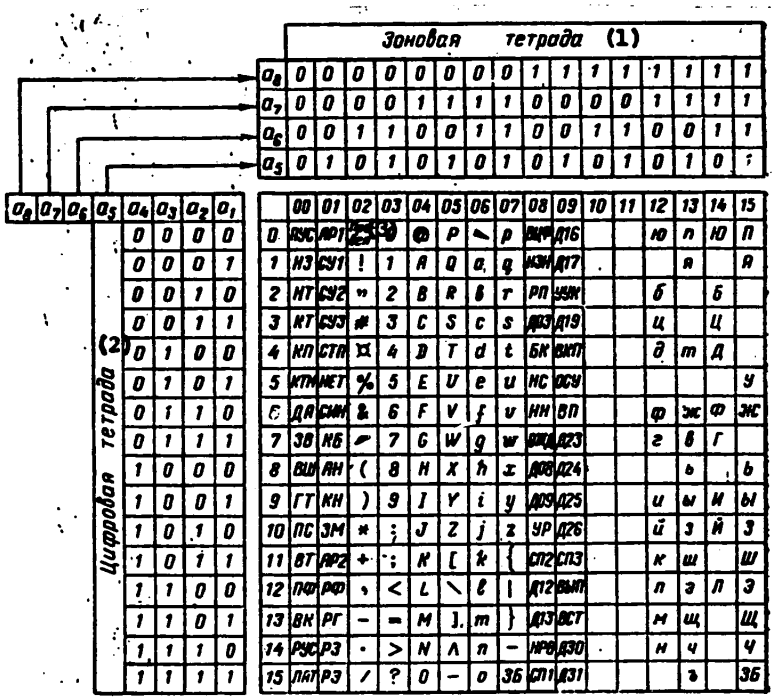

Figure 2.2. Code Table of Eight-Bit Information Exchange and Processing Code (KOI-8)

Key:
1. Zone tetrad
2. Digital tetrad
3. Space

The DKOI is designed to process information in machines. It is convenient for placing information on punch cards. The KOI-8 and DKOI code tables are shown in Figures 2.2 and 2.3, respectively.

As can be seen from the tables, there is no register division in them. The bits of the code combination are denoted by the letters a_8-a_1 in the KOI-8 and by the numbers 0-7 in the DKOI. The letters and numbers indicate the ordinal numbers of bits in the code combination and correspond to the following weights:

Биты в КОИ-8 (1)	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1
Биты в ДКОИ (2)	0	1	2	3	4	5	6	7
Веса (3)	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Key:
1. Bits in KOI-8
2. Bits in DKOI
3. Weights

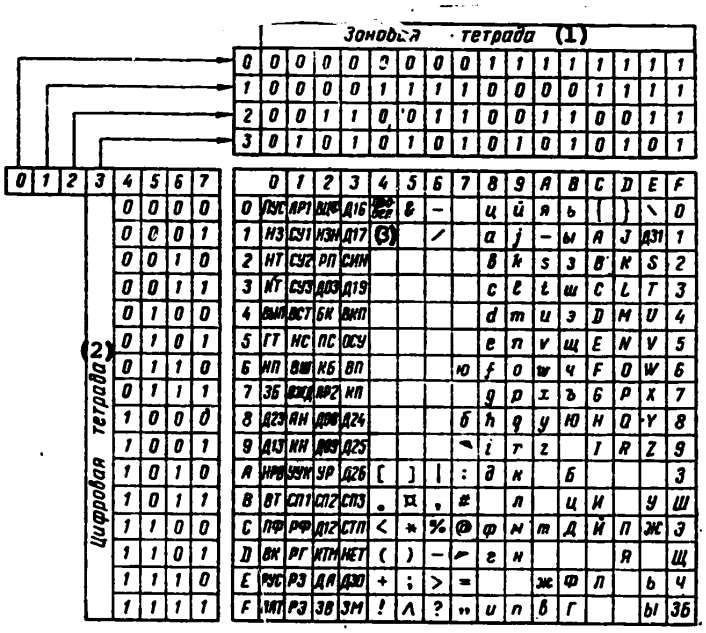

Figure 2.3. Code Table for Binary Information Exchange and Processing Code (DKOI)

Key:

1. Zone tetrad
2. Digital tetrad
3. Space

The encoding byte is divided into tetrads. The four most significant bits of the code combination depicted above the ordinal number of the table column (a_8-a_5 in KOI-8 and 0-3 in DKOI) are the zone tetrad while the four least significant bits located alongside the ordinal number of the row (a_4-a_1 and 4-7) are the digital tetrad. The first two most significant bits of the DKOI in the zone tetrad determine one of the zones:

00 -- zone of service symbols;
01 -- zone of graphical symbols;
10 -- zone of lower case Latin and Russian letters;
11 -- zone of capital Latin and Russian letters and numbers.

The next two most significant bits, along with the first, determine the column in which the symbol is located. The bits of the least significant digits of the byte finally determine the address. Any symbol of 256 code combinations is determined by the code position (a fraction whose numerator is the column number and whose denominator is the row number) and also by a code combination--the code. For example, the code of the capital letter E is determined:

by a fraction--04/5 (KOI-8) and C/5 (DKOI);

by the code combination--01000101 and 11000101.

The code for the symbol KT (end of text) will be determined as 00000011 (for KOI-8 and DKOI) by the same rules.

The machine word of the KOI-8 will be encoded by five bytes and written in the machine memory in the following form:

	К	О	И	—	8
КОИ-8	—01001011	01001111	11101001	01011111	00111000
ДКОИ	—11010010	11010110	11001011	01100000	11111000

2.2. Information Carriers

An information carrier is understood in the general sense as the physical medium which is used to record and store information.

The basic economic information carriers are the primary documents in which all the economic operations completed by an enterprise or organization are reflected. They include different requirements, overhead, orders, interchangeable certificates and so on. However, primary documents are mostly suitable for use by man but are not suitable for direct computer entry of data from them. Therefore, the information from them is first placed on intermediate machine carriers in codes suitable for computer processing using data preparation devices. Punch cards, papertapes, magnetic tapes, cards, drums and disks are used as the machine carriers of information. Besides these carriers suitable only for use in computers, carriers that combine primary documents and machine carriers, which are suitable for simultaneous use by man and computers, find application. They include machine-readable documents--dual-cards, standardized forms the information from which is read directly by means of automatic reading machines, punch cards with graphical marks and so on.

Let us consider the basic machine carriers and methods of encoding information on them.

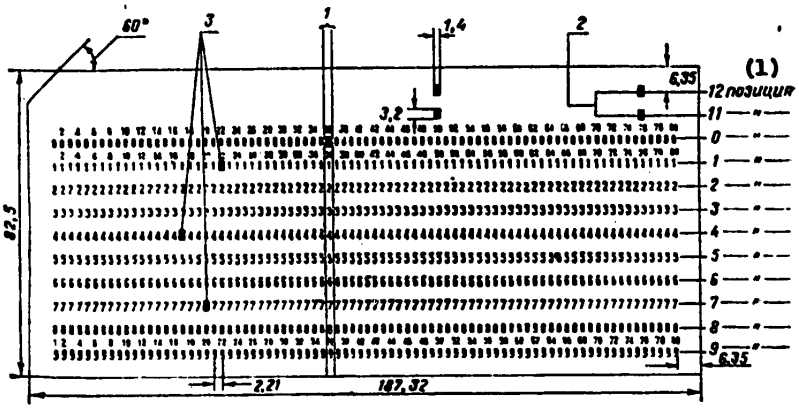

Figure 2.4. 80-Column Punch Card (PK80)

Key:
1. Position

The punch card is a rectangular paper card measuring 187.32 X 82.5 mm (GOST 6198-75), manufactured from punch card paper (0.18 mm thick with tolerance of ± 0.01 mm. The upper left hand corner of the punch card is cut at an angle of 60° for convenience in stacking it into files. The remaining corners of the punch card can be straight or rounded for greater wear resistance.

Two types of punch cards are now employed--45-column (PK45) and 80-column (PK80). Eighty-column punch cards having higher recording density are mainly used in computers (Figure 2.4).

The numerical matrix imprinted on the front side of the punch card separates it into vertical rows--columns 1 and horizontal rows--positions (lines) 12-9. Besides the 10 positions denoted by numbers, there are additional 11th and 12th positions not denoted by numbers in supernumerical field 2. The information intended for imprinting on the punch card (input data and programs) is written on forms in octal or decimal counting systems. It is then transferred to the punch cards in the form of perforators 3 located at the intersection of a position and column by using data preparation devices. In this case the perforation corresponds to code 1 and the absence of a perforation corresponds to code 0. The perforations may be numbers, letters and special symbols which are automatically read and transferred to the computer memory.

According to GOST 6198-75, 80-column punch cards are manufactured in the following types:

PK80--with complete numerical grid;

PK80N--with incomplete numerical grid;

PG80/27--with zone for graph marks (one-sided);

PG80/54--with zone for graph marks (two-sided).

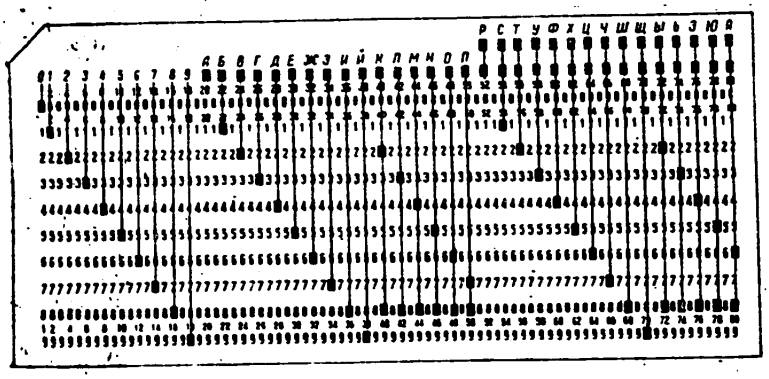

Figure 2.3. Encoding of Alphanumeric Information in Decimal Counting System According to GOST 10859-64

Numbers are printed only in positions 0, 3, 6 and 9 in punch cards with incomplete numerical grid, which permits auxiliary inscriptions on the front side of the punch card. The arrangement and dimensions of the perforations in punch cards should correspond to GOST 8912-76.

Rectangular holes are punched with base of 1.4 mm and height of 3.2 mm in an 80-column punch card. The distance between the centers of the perforations in two adjacent columns (the spacing between columns) is 2.21 mm. The distance between the centers of two adjacent perforations in a single column (spacing between positions) comprises 6.35 mm. The maximum number of perforations which can be placed on an 80-column punch card is 960 (12 X 80).

The information on punch cards can be arranged by columns (in Minsk and YeS computers) or by position on lines (in BESM and Ural computers). According to GOST 10859-64, information can be inserted in decimal or binary number systems. One symbol usually occupies one column with this arrangement. The code of GOST 10859-64 permits one to encode no more than 128 different symbols. It is made up so that any symbol in the column is depicted by an odd number of perforations (1, 3, 5, 7), which is necessary to check the correctness of data entry into the computer. The zero position of the punch card serves as a supplement to oddness.

The punch cards are inserted in the reading device by the narrow side with column arrangement of information. Representation of information in the decimal number system is used extensively when processing economic information.

Encoding of alphanumeric information on an 80-column punch card in the decimal number system according to GOST 10859-64 is shown in Figure 2.5.

If the information is arranged by position (by line), one symbol occupies from three to eight columns of a single position (line) depending on the type of information. The punch cards are inserted in the reading device by the wide side.

The 12-position KPK-12 punch card code with column arrangement of symbols is used in the YeS EVM to enter information on the punch card. The KPK-12 code table is presented in Figure 2.6. The table is divided into two parts--a left part (columns 0-7) and right part (columns 8-15). The code combinations that indicate the numbers of the positions in the punch card in which perforations should be made are presented in the extreme left hand and right hand columns and also in the top row of the table.

Letters of the Russian alphabet, similar to Latin letters, have the code of Latin letters. Instead of the symbol (code position 1/15), the symbol is permitted. The capital letter Ъ is permitted in code position 7/7. Any symbol of 256 code combinations is determined by the code position (the fraction whose numerator is the column number and whose denominator is the row number (and also by the code combination--the code. For example, the code of capital letter Щ is determined:

by fraction 15/11;

by code combination--12-11-0-9-8-3.

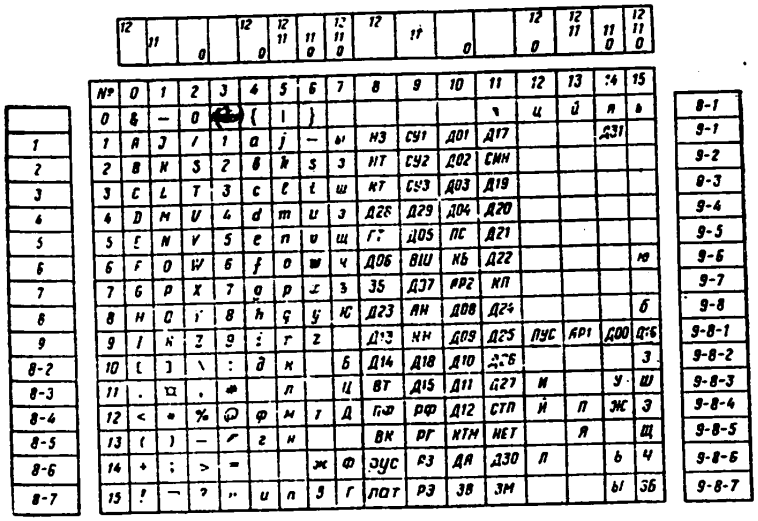

Figure 2.6. Code Table of 12-Position KPK-12 Code

Key:

1. Space

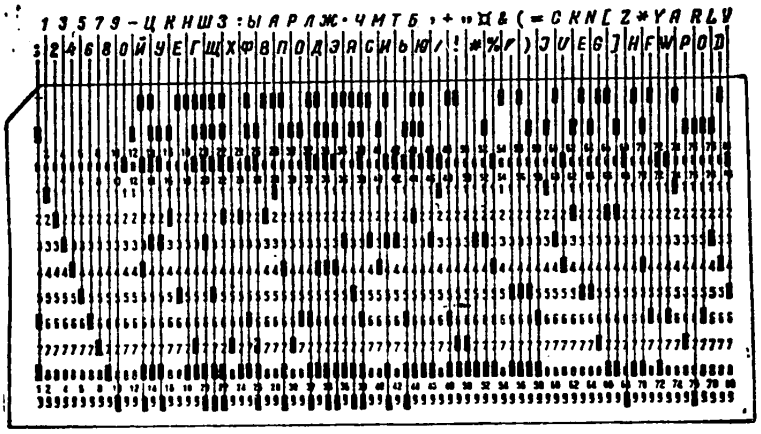

Figure 2.7. Representation of Alphanumeric Information in KPK-12 Code

Representation of information in KPK-12 code is shown in Figure 2.7. The extensive use of punch cards as information carriers is explained by their advantages:

high strength and long storage time;

convenience of making corrections to errors by punching new cards;

the capability of creating a large capacity of permanent card files;

convenience of grouping by features and retrieval of the required information;

The disadvantage of punch cards is the limited recording density (80 decimal digits) and the speed of reading information (300 punch cards per minute when fed by the narrow side).

Papertape is a narrow tape 0.1-0.15 mm thick manufactured from high-quality sulfate or waxed paper. Tapes of increased strength manufactured from plastics are also used.

Information is entered on the papertape by punching round holes arranged along the code tracks (positions). Five-, six-, seven- and eight-track tapes are used. The perforations in the transverse direction form rows. A single symbol corresponding to the code of a number letter or sign is written in each row. The maximum number of different symbols which can be placed on a papertape depends on the number of coding tracks which in turn determine the type of code used. For example, up to 32 symbols (2^5) can be written on a five-track tape and up to 256 symbols (2^8) can be written on an eight-track tape.

Three types of code--the second international code MTK-2 intended for data transmission over communications lines, GOST 10859-64 code used mainly to enter information in a computer and KOI-7 code (GOST 13052-74), which is unified for entry of information into the computer and transmission of it over communications lines.

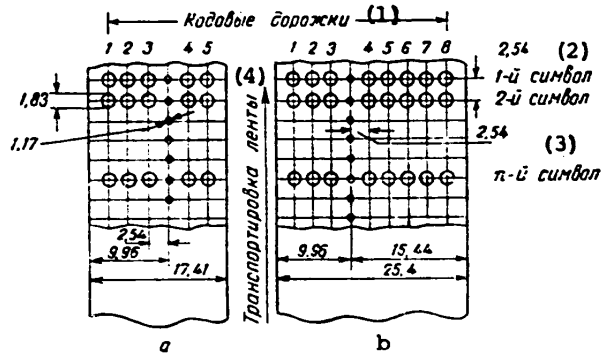

Figure 2.8. Arrangement of Information on Papertape According to GOST 10860-68: a--five-track papertape; b--eight-track papertape

Key:
1. Code tracks
2. Symbol
3. n-th symbol
4. Tape transport

KOI-7 code, whose table is presented in Figure 2.1, is used in YeS computers. Seven bits of this code are arranged on the seven code tracks of the papertape, while the eighth track is used to punch the eighth control bit, which supplements the

code combination in the row to an even number of digits. Besides the main (code) tracks, there is an additional synchronizing track in which smaller diameter holes are punched. The dimensions, shape and arrangement of the holes of five- and eight-track papertapes according to GOST 10860-68 are shown in Figure 2.8 and information coding on an eight-track papertape in the YeS computer is shown in Figure 2.9.

The advantages of papertapes are: high rate of entry (up to 1,500 lines per second), capability of recording information of any length, storage convenience, low cost and capability of automatic entry of information when compiling documents on tabulating computers and recording information received over communications channels.

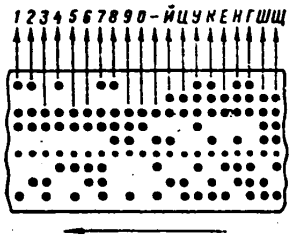

Figure 2.9. Information Coding on Eight-Track Papertape in YeS Computer

The disadvantages of papertape should include low strength and difficulty of correcting errors and also no capability of preliminary grouping of information. However, because of the advantages noted previously, papertape is one of the most widely used information carriers.

Magnetic tape is a plastic or polyester tape coated with ferromagnetic material.

Information is recorded on a magnetic tape and the recorded information is read by means of a magnetic head when the tape moves over it (see Chapter 8 for more details).

Magnetic tapes have different width and different number of tracks. The width of a standard tape is 12.7 mm. Its length in the reel comprises 125-1,000 meters.

Information is recorded or read in groups of words arranged in specific zones having their own number. The numbers of the zones, instructions and numbers are recorded on code tracks. Information is recorded and read by the magnetic head unit located along the code tracks. The recording and reading speed comprises 10^4-10^5 or more characters per second. Recording density is 8-64 bits/mm.

The shape and arrangement of tracks on a magnetic tape 12.7 mm wide are shown in Figure 2.10. A total of nine tracks are located on the tape, of which eight are information tracks and one (the fourth from the base edge) is a control track which is used to check the correctness of information transmission by evenness. Recording of binary symbols on the tracks is shown arbitrarily.

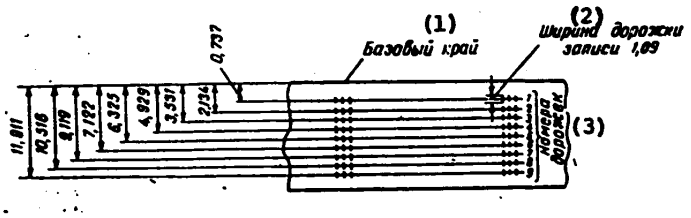

Figure 2.10. Shape, Dimensions and Arrangement of Recording Tracks on Magnetic Tape According to GOST 12065-74

Key:
1. Base edge
2. Width of recording track 1.09
3. Number of tracks

Magnetic tapes have found broad application in modern computers as large-capacity external storage devices. Their sphere of utilization was expanded considerably with the appearance of keyboard data recording devices. Magnetic tapes became carriers for direct entry of information into computers. The high density and information recording and reading speed are a considerable advantage of magnetic tapes over other machine carriers. Their main disadvantage is the lack of capability of visual reading of information and insufficient strength.

Magnetic cards. A magnetic card is a plastic card manufactured from a polyester base to which is applied a magnetic layer coated on the top with a protective layer of polyester film. The recording and reading speed is 20,000 characters per seconds. Recording density comprises 10 binary characters per millimeter. Information is recorded on several tracks. The number of tracks depends on the dimensions of the magnetic card: a card measuring 366 X 82.5 mm has 56 tracks and one measuring 76.2 X 25.4 mm has 21 tracks. The capacity of each of the cards comprises 130,000 and 4,500 binary characters, respectively. For comparison let us point out that the average capacity of a punch card is approximately 5,000 characters.

The information characters considered above should provide rather rapid entry of data into computers, simple checking of the correctness of information entry and the capability of checking the information during processing, including visual checking, to arrange it in order and to replace it if necessary. Besides printout on an ATsPU (alphanumeric printer), intermediate and resultant information should be recorded on one of the carriers. The experience of developing information files shows that organization of the production process of carrier preparation and their adaptability to making changes and modifications must be taken into account when selecting an information carrier, along with its capacity.

Punch cards with zones for graphic marks. The punch carriers (punch cards and papertapes) considered earlier have a significant disadvantage--the labor expenditures to prepare them comprise 90 percent of the entire expenditures for machine processing of information. This is related to the fact that information is transferred to these carriers by manual setting of it on the keyboard of special data preparation devices.

Cards with graphic markers are used to automate the information process. This card is a standard 80-column punch card on which zones for graphic markers are designated typographically.

Punch cards are manufactured in two types: those with zones for marks on the front side (PG 80/27)--one-sided--and with zones on the front and back side (PG80/54)--two-sided. The zones of each side of the punch card are 27 oval columns, each of which occupies three columns. Entry of information on this card reduces to shading the ovals with soft pencil or light-conducting pens. Information is read from the punch cards automatically by means of reading perforators. A total of 27 marks can be read and 27 perforations can be punched from a one-sided punch card during one pass of the card through the machine, while 54 marks can be read and 54 perforations can be made with a two-sided card. The reading speed is 100-120 punch cards per minute. During reading the cards move by positions; therefore, the number of columns during reading and perforation does not affect the productivity of the machine.

Machine-readable documents--these are documents for automatic readout of information--are a combination primary document and machine carrier. These documents are dual-cards and standardized forms for automatic reading machines.

A dual-card combines the functions of primary document and punch card. The form of the primary document is entered on it typographically. The requisites, i.e., the information model, are indicated in the supernumerical field.

Permanent characters are punched by duplication from previously prepared permanent papertape. The volume of this information, as shown by experience, comprises 75-80 percent of the total volume of data.

The variable characters and qualitative indicators are recorded in dual-cards by means of graphic markers which are read automatically by means of reading perforators.

The use of dual-cards permits almost complete automation of the perforation process.

Standardized forms are used for direct readout of information by using automatic reading machines. The information is recorded on forms in a code convenient for perception by the machine. Information is recorded by means of graphic markers with normalized and stylized types.

Information is recorded in normalized types by hand in special rectangles imprinted on the form typographically. Several normalized types have been developed. They may include a type for the Ruta-701 automatic reading machine, which is entered in the rectangles measuring 5 X 3.5 mm. A total of 10 numbers and 4 service characters can be entered on the form by using this type. They also include a type for encoding postal addresses on envelopes.

Stylized types include type which comprises code elements of each alphabet character. An example of it is SMS-7 magnetic stylized type which is entered on forms by a typewriter keyboard and magnetic tape impregnated with magnetic ink.

It should be noted that standardized forms, due to their limited dimensions, requirement of high strength of the paper and complexity of the information input and readout devices, have still not found wide application.

The method of transferring information onto magnetic carriers when filling out documents is now used extensively to automate carrier preparation processes. The hardware that implements the indicated method includes bookkeeping and billing machines outfitted with special attachments. A papertape, punch card or magnetic tape can be produced as the machine carrier during their operation.

Information is automatically recorded on machine carriers also during transmission over communications channels and also when using different production recorders and special data preparation systems of type SPD-9000.

2.3. Devices for Data Preparation and Rewriting Information from One Carrier to Another

Information is now entered into modern computers mainly from punch cards, papertape and magnetic tapes. Data preparation devices based on punch cards, papertapes and magnetic tapes are used to prepare these carriers.

Punch card data preparation devices (UPDK). They are a perforator designed to apply perforations onto punch cards according to an established code.

The composition of the UPDK is different for individual types of computers. Thus, for example, cards are prepared for the Minsk-32 computer by means of the UPDK-32 in GOST 10859-64 code. The UPDK-32 includes a Konsul-254 typewriter and P80-6 perforator.

The following devices are used in the YeS computer to prepare cards: YeS-9010 (USSR), which is used to enter information on punch cards with simultaneous printing on a roll or form, the YeS-9011 (USSR) designed to make perforations on punch cards and to decipher the information of each column on the upper field of the card, and the YeS-9012 (USSR) which combines the functions of perforator and checking-reading device.

The PA80-2/3M keyboard perforator and the KA80-2/3M verifier.

The PA80-2/3M perforator is designed to enter digital information in KTK-12 code on 80-column punch cards. It is single-period, i.e., the holes are punched simultaneously when the keys are pressed.

The following can be carried out on the perforator: manual perforation of a set of numbers, letters and characters, passing a punch card by one column without perforation (single skipping), passing a punch card by several columns without perforation (multiple skipping), complete skipping of a punch card from any column without perforation (ejection of punch cards), automatic perforation of permanent characters from a master card, automatic perforation of a series of identical punch cards from a master card and perforation in one column of any code combination with up to eight perforations. The speed of manual perforation is 12 columns per second.

The perforator has two keyboards--alphanumeric and numeric. Combination keyboards of the Russian and Latin alphabets, numbers and characters, are arranged on the panel of the alphanumeric keyboard, while 12 keys, of which 10 are numeric (0-9) and two are control holes (11 and 12) are arranged on the panel of the numeric keyboard. Each keyboard has three control keys.

The numeric keyboard permits perforation in two modes: single- and two-period. In the first case perforations are made and the card is moved to the next column by pressing on the key once. In the second case perforations are punched and the card is moved during two cycles--the set of information is collected during the first cycle and perforation and movement of the card are carried out during the second cycle. The two-period mode permits information to be entered in a single column in any code.

The PA80-2/3M perforator consists of 12 punch solenoids and a matrix with 12 dies. When the key is pressed, the corresponding solenoid is triggered whose armature lowers the die located in the die groove by means of a lever. The die, when lowered, punches holes in positions corresponding to the code being used.

The KA80-2/3M verifier is designed to verify the correctness of entering the information on punch cards. Performation is verified by comparing the perforations in punch cards with the data of primary documents.

The verification technique is similar to perforation with the only different that verification of holes rather than perforation of holes is carried out on the verifier. In this regard the perforator has been replaced by a reading device which consists of a contact block and reading unit with 12 brushes. The remaining devices of the verifier are similar to the perforator. If the numbers of the pressed key coincide with the perforations in a given column, the punch card is moved to the next column and if they do not coincide it stops and a signal lamp lights up.

The YeS-9013 (USS) and YeS-9018 (CSSR) devices are also used to verify the correctness of perforation. The distinguishing feature of the YeS-9018 verifier is the use of a storage device. Data entered on the punch card are read and stored in the memory. These data are entered from primary documents by means of a keyboard and are compared to the data in the memory. An error signal is triggered if there is disagreement. Reading speed is 290 columns per second.

Other machines such as the following, for example, may also participate in preparation of punch cards for further processing of them.:

reproducer-perforators--for reproduction of cards (producing copies from each punch card of the file) and also for duplication (production of several copies from a single master card);

sorting machines--for grouping cards according to given features;

decoding machines--to print information entered on punch cards and other machines.

For example, the YeS-9014 device--a punch card column decoder (CSSR), which automatically decodes the data entered on the punch card and prints the characters of each column on the upper edge of the punch card--is used in data preparation for the YeS computer. The data punched on the punch card is read by a program card and recorded in the memory, while the characters are printed by columns with continuous movement of the punch cards at a speed of 60 columns per second.

The YeS-9015 device--a decoder-perforator (CSSR), which prints data along the edge of the card simultaneously with entry of alphanumeric data on the punch card--is used for the same purpose.

Data is initially entered from primary documents by means of a keyboard into the computer memory, the data are punched on the card after the memory has been filled for one punch card and are simultaneously printed on its upper edge at a speed of 60 columns per second.

The data along the edge of the punch card are decoded simultaneously with perforation and verification in the YeS-9080 punch card data preparation device (CSSR).

Papertape data preparation devices (UPDL). They are a perforator designed to make perforations on papertape according to an established code.

The tape perforators, depending on the width of the tape, have different design. For example, STA-2M and STA-5M telegraph apparatus serve as tape perforators when using five-track telegraph tape 17.5 mm wide.

The tape perforator for the Minsk-32 computer is the Brest-1 UPDL device.

The YeS-9020 device, which includes the following, is used in YeS computers to prepare eight-track papertape 25.4 mm wide:

a Konsul-260 typewriter with set of symbols for perforation;

PL-80 tape perforator to make perforations on papertapes;

reading unit to read information from two papertapes and to transmit it to the verifier;

verifier unit to compare the papertape codes and to transmit them to the tape perforator.

THe YeS-9020 device operates in several modes:

a) punching holes in papertape with the typewriter keyboard and printing information on a form (the data preparation mode);

b) reproduction of the papertape (the reproduction mode);

c) comparison of the information entered on two papertapes (the comparison mode);

d) verifying the information on the papertape by comparison with information assembled on the keyboard (the keyboard comparison mode);

e) comparison of two papertapes to the perforation of a third tape in the case of code conformity (reperforation comparison mode);

f) comparison of two papertapes to the perforation of a third tape and printing the information on a form (the comparison and printing mode).

The information processing rate is from 10 to 50 characters per second.

YeS-9021, YeS-9022 (CSSR) and YeS-9024 (USSR) devices are also employed for data preparation on papertape.

The distinguishing feature of YeS-9021 and YeS-9022 devices is the presence of a display and the capability of the tape perforator and reading device to work with cards with edge perforation.

The YeS-9024 device permits one to perform a number of additional functions: retrieval of a given code, stopping according to the code, automatic skipping of "failure," "empty" codes and so on.

2.3.1. Magnetic Tape Data Preparation Devices (UPDML)

These devices are designed for data preparation on magnetic tape for further processing on YeS computers.

The YeS-9001 device (USSR) operates in two modes:

a) recording on tape the data entered by an operator by means of an alphanumeric keyboard;

b) printing data read from magnetic tape when the device is connected to a typerwriter.

The device consists of a magnetic tape unit, control unit with buffer memory and alphanumeric keyboard. It performs the following operations:

entry of program and data input;

data and program retrieval;

data verification;

data and program output.

The data formation program is entered in the device from a keyboard or magnetic tape. The entered data, their formation and storage are verified in the buffer memory of the control unit.

After the last character of the data unit has been entered, information is re-recorded from the buffer memory to magnetic tape in the form of a zone and then the correctness of recording on the magnetic tape is verified automatically. After the entire data file has been entered, the device is converted to the verification mode during which the data entered from the document are compared to the data read from the magnetic tape. If there is disagreement the data on the magnetic tape are corrected in the correction mode.

The device permits entry of up to 96 characters. Recording density is 8 bits/mm. Information is transferred to magnetic tape in DKOI code. The maximum length of the zone is 180 characters. The speed of composing the characters on the keyboard is 20 characters per second.

The YeS-9002 device (Peoples Republic of Bulgaria) is designed for direct recording on magnetic tape of information entered from a keyboard. The device permits verification and if necessary correction of the data recorded on the tape. It has a built-in buffer memory.

The main operating modes are program entry, program verification, data entry, data verification, retrieval of data unit, entry and verification of entered data to buffer memory and reading of data from buffer memory.

Information is recorded on magnetic tape, as in the YeS-9001 device, after the last character of the data unit has been entered. After the data unit has been recorded, the tape is rewound the length of one unit, after which it again begins to move forward. During the second movement, the data reproduced from the tape are compared to the data in the memory. The alphanumeric display permits one to follow the information being entered or verified.

Data are composed from the document a second time in the "DATA VERIFICATION" mode after the data unit has been played back and entered in the data memory. The character code is automatically compared in this case to the code in the memory. If both codes are identical, the operator can continue to verify the data.

The desired data unit is retrieved automatically in the "DATA UNIT RETRIEVAL" mode by comparing the data played back from the tape to an identifier recorded in the data memory by means of a keyboard.

The device has the following specifications: recording density of 32 bits/mm, magnetic tape speed of 39.6 cm/s, buffer storage capacity of 200 bytes and length of recording unit of 80 or 160 bytes. A block diagram of the YeS-9002 device is shown in Figure 2.11.

The YeS-9006 device (Hungarian Peoples Republic) is a plug-in magnetic tape data preparation system.

Data is recorded from primary documents onto a plug-in magnetic tape by using an alphanumeric keyboard. Data can also be entered from the integration unit or from the plug-in package on which the program is recorded. The recorded pack is verified by second entry of data from the keyboard. The system includes a pack type magnetic tape store and operator console. The capacity of the pack is 80 Kbytes

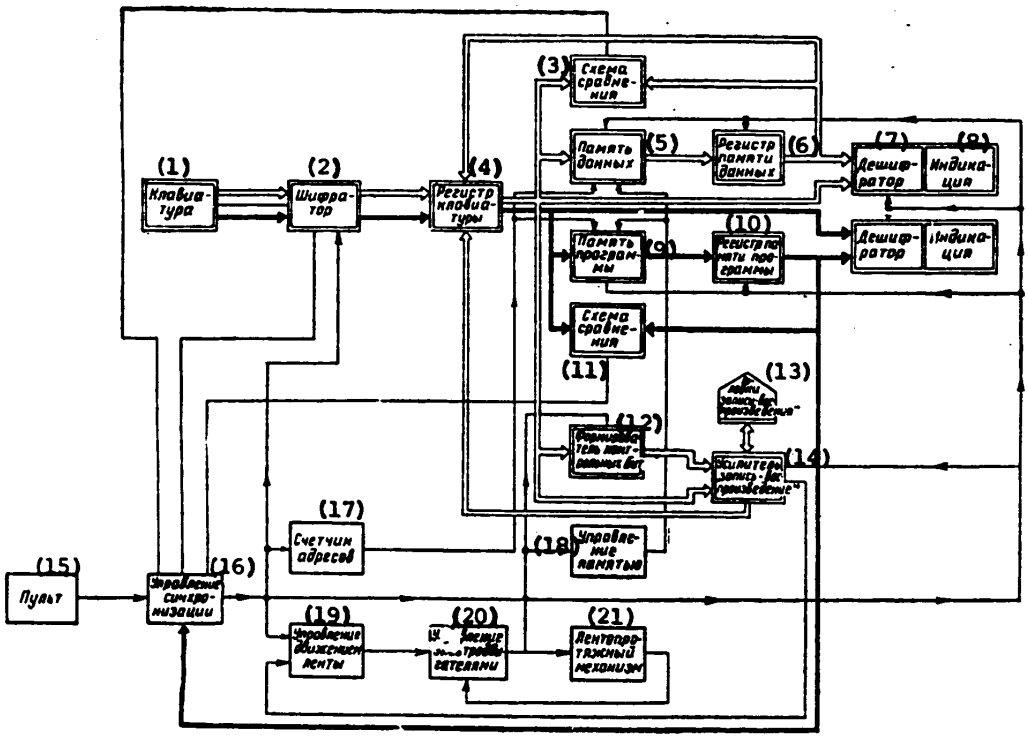

Figure 2.11. Block Diagram of YeS-9002 Magnetic Tape Data Preparation Device

Key:

1. Keyboard
2. Encoder
3. Comparison circuit
4. Keyboard register
5. Data memory
6. Data memory register
7. Decoder
8. Display
9. Program memory
10. Program memory register
11. Comparison circuit
12. Verification bit shaper
13. "Record-playback" unit
14. "Record-playback" amplifier
15. Console
16. Synchronization control
17. Address counter
18. Memory control
19. Tape feed control
20. Electric motor control
21. Tape feed mechanism

(on each side). The digit capacity of the unit is 80 characters. The average data transmission speed is 140 bytes per second.

Devices for rewriting information from one carrier to another. IBMs differ by the capability of receiving information from different machine carriers. This circumstance made it necessary to develop devices to rewrite information from type of carrier to another.

As an example, let us consider a device for rewriting information from papertape to punch cards (BLP-1). This device provides rewriting of information from five-, six- and seven-track papertapes to 80-column punch cards with conversion of the papertape code to the alphanumeric code of the punch card with symbol encoding by no more than two perforations in a column or to binary code for 64-code combinations with position arrangement of symbols on the punch card and automatic verification mode by comparison of the perforated punch card file to the papertape. The input speed is 200 characters per second and output speed is 115-120 punch cards per minute.

The corresponding rewriting devices can also be used to transfer information from punch cards or papertapes to magnetic tape if the latter is used to enter data into the machine.

Devices for rewriting from punch cards to papertape are used extremely rarely with regard to the fact that almost all computers have punch card input.

Chapter 5. Central Processor

5.1. Block Diagram of Processor

The central processor (TsP) is a calculating device in which program instructions are realized and in which all the assemblies of the computer system interact. The central processor includes devices for access to the internal storage in which the program written in machine language is stored. The processor is connected to peripheral devices through input-output channels as needed.

Functionally, the processor is the central device of the computer system. It includes:

a central control device (TsUU);

arithmetic-logic device (ALU);

high-speed memory (SOZU);

internal storage control unit (BUOP);

apparatus for communication of the central processor with peripheral devices;

control console (PU).

The internal store (OZU) and channels for communication with peripheral devices are performed in computer systems in the form of independent units. But in some low-productivity computers, for example, in the YeS-1020 computer, the communications channels and internal storage (OP) are contained in the processor.

The central processor fulfills programs by sequentially implementing machine instructions in the order given for them. In this case the central processor fulfills

only those programs which are stored in the internal storage. A block diagram of the processor and communication of it with the internal storage are presented in Figure 5.1. Communication between the TsUU, ALU and OP are provided by two information mainlines--number code buses (KShCh) and address code buses (KShA).

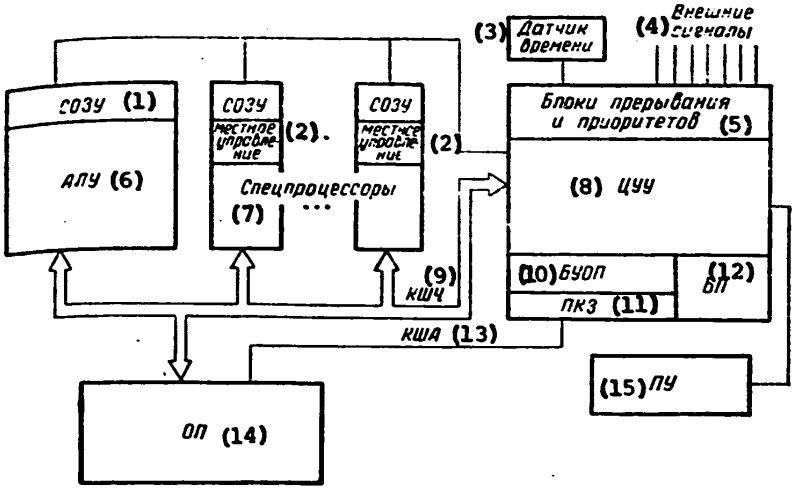

Figure 5.1. Block Diagram of Central Processor

Key:

1. High-speed storage
2. Local control
3. Time sensor
4. External signals
5. Interrupt and priority units
6. Arithmetic-logic device
7. Special processors
8. Central control device
9. Number code buse
10. Internal storage control unit
11. PKZ
12. Buffer storage
13. Address code bus
14. Internal storage
15. Control console

The central control device receives instructions from the internal storage, decodes instruction codes, generates control signals to fulfill these instructions, calculates operand addresses (numbers and machine words) and ensures that the order of following the program instructions is adhered to.

The central control device, besides units used to receive and decode instructions and also the synchronization unit, includes units that provide multiprogram operation of the computer system: interrupt and priority unit, memory security unit, time sensor and so on.

Arithmetic operations on numbers with fixed and floating point, logic operations and operations on machine words of variable length are carried out in the arithmetic-logic device.

Several special processors are shown in the central processor in Figure 5.1, which is typical for third-generation computers in which it was planned to separate functions of information processing inside the central processor. For example, units for operations on binary numbers with fixed point, binary numbers with floating point, for processing decimal numbers and so on can be provided.

A high-speed store is included in the processor to increase its speed. The SOZU is usually fulfilled on registers (high-speed register memory) having direct addressing. The register addresses indicated in the program do not require any processing at all, which considerably reduces the access time of operands from the SOZU compared to the access time from the internal storage.

The SOZU stores machine words of fixed length subject to processing during current operations, intermediate results of calculations, values of indices used for re-addressing and also individual sections of programs which should be carried out in the near future.

The internal storage control unit (BUOP) provides interaction of the central processor units and channels with the internal storage. All access to the internal storage from the central processor and channels are provided according to priorities.

It should be noted that a considerable fraction of funds and time go to work to develop the processor--an increase of its speed and improvement of its engineering and operational characteristics--during development of first- and second-generation computers.

A great deal of attention is now being devoted to problems of integrating external devices with the central processor and internal storage and of organizing the functioning of the computer complex as a whole.

The characteristic feature of third-generation computer development is development of computer systems that include a number of models differing from each other in productivity. The productivity of the YeS computer fluctuates from 20,000 to one million operations per second, which is determined mainly by the principles of designing the processors of these models.

Models of the YeS computers have very significant differences in the makeup and working principle of the arithmetic and logic units. As is known, the basis of the ALU is the adder in which both arithmetic and logic operations are realized. Like other computer assemblies designed to fulfill instructions (operations), the adder comprises the operational part of the ALU. The operational part of the ALU of the YeS-1050 model includes two units--the arithmetic adder unit (BAS) and the digital decimal arithmetic unit (BATs). The basis of the BAS is a parallel-operating 64-digit binary adder in which the operands of all fixed formats (from a half-word to a binary word) can be processed. The decimal numbers in the eight-digit decimal adder are processed in the BATs. An eight-digit logic switch is provided in the BATs to perform logic operations on fields of variable length.

The operational part of the ALU of the YeS-1030 model includes a 32-digit adder (SM) in which operations are performed on binary and decimal numbers and an

assembly for logic processing of information (UOB) in which logic operations on the operands of fixed and variable length are performed and the orders of operands with floating point are also processed.

Arithmetic and logic operations are performed in the YeS-1020 model in a combination type universal arithmetic-logic unit (ALB). The operations provided by the instruction system of YeS computers are realized in the ALB by different switches of the combination circuit; therefore, the same electonic assemblies comprising the ALB can perform arithmetic and logic operations and also operations with operand addresses.

It is obvious from the brief survey of the arithmetic-logic devices of the YeS-1050, YeS-1030 and YeS-1020 computers presented above that the use of units with different functional designation in the ALU is typical for the more productive YeS-1050 computers, while the universal nature of the assemblies comprising the ALU is typical for low-productive computers.

The program compatibility of all models of YeS computers includes the capability of performing all arithmetic and logic operations, assembly of which is determined by the instruction system of the YeS computers, but the characteristic features of designing different models of central processors required a different approach to realization of algorithms of the same operations in different models.

The characteristic features of designing arithmetic and logic devices and also of realizing arithmetic and logic operations in the ALU of different models of YeS computers are considered in detail in 5.6. The number of bytes simultaneously accessed from the internal storage (access width) is different for computer models of the unified system, which is considerably reflected in the speed of the computers. For example, the access width in the YeS-1020 computer is two bytes, it is four bytes in the YeS-1030 and eight bytes in the YeS-1050 computer. Accordingly, the instructions containing 4 or 6 bytes are accessed from the internal storage in two or three accesses in the YeS-1020 computer, while two instructions containing 4 bytes each (RX, RS and SI formats) or four instructions containing 2 bytes each (RR format) are selected in one access to the internal storage in the YeS-1050 computer. An increase of the access width reduces the time required to perform an operation, but requires that the apparatus be more complicated. Thus, for example, 8- and 16-digit registers are mainly used in the YeS-1020 computer, 32-digit registers are used in the YeS-1030 computer and 64-digit registers are used in the YeS-1050 computer, which provides different methods of reception, arrangement and handling of data in different models.

The models of computers in the Unified System differ by control principle: the microprogram control principle is used in the YeS-1020, YeS-1030 and YeS-1040 and the circuit (with "rigid" logic) is used in the YeS-1050 and YeS-1060 computers. The principle of control with "rigid" logic provides higher speed but requires more complex apparatus solutions, which results in making the model more expensive. The difference of the control principles is considered in more detail in 5.3.

Models of the YeS computers have different capabilities for integration of individual functional assemblies during operating time. The level of integration of individual operations of older models of the system, having greater apparatus

composition is higher than the younger models, which determines the speed of the model. For example, the YeS-1020 and YeS-1030 models, having identical component base and microprogram control devices, differ from each other in speed due to the different level of integration of performing operations.

The two main devices of the central processor--the arithmetic-logic device and the central control device--are considered in more detail below.

5.2. The Central Control Device

The central processor control device, or central control device (TsUU), is one of the basic devices of a computer and is designed to automatically carry out the programs in the computer.

The central control device generates the main signals required to perform all operations provided by the instruction system and also provides coordinated operation of all assemblies and units of the computer. The central control device controls all operations which are performed in the computer memory, the arithmetic-logic device, in external device communication channels and in the external devices themselves. Besides the central control device, the computer system may have local control devices that generate additional control signals.

As was mentioned above, computers utilize the program principle of control which ensures automatic control of all the units of the machine. The program includes a sequence of instructions that determine the order of actions which should be performed to solve a problem.

The program is entered in the internal storage of the computer prior to the beginning of work, from which instruction after instruction is sequentially selected during problem solving. Input data subject to processing by this program are entered in the internal storage simultaneously with the program.

The order of following the instructions in the program can be given in explicit or implicit form. The address of the next instruction is given with explicit assignment of the order of tracking in the address part of the instruction, besides the operand addresses. The order of following instructions is called forced.

More widespread in computers is the implicit order of assigning instruction addresses when the instructions are arranged in the internal storage one after the other in an order determined by the problem algorithm. This method of instruction addressing is called natural. The location of program arrangement in the computer is determined when it is loaded into the internal storage and the beginning of the program is controlled by the basic address. Access to the program can be gained from the control console of the machine or automatically.

Each instruction (operand) occupied the same memory cell in first- and second-generation computers and therefore the routine instruction addresses were determined by adding a 1 to the least significant digit of the contents of the instruction address counter (the instruction address counter stores the address of the current instruction over the entire time of fulfilling it).

The routine instruction address is determined in third-generation computers by adding the address of the current instruction and the number of bytes that determine the length of the instruction to be fulfilled. The number of bytes contained in the instruction is indicated in the most significant bits of the operation code and it is retransmitted to a special register of the control device at the moment the instruction is fulfilled. To find the address of the next instruction, the contents of the instruction length register are added to the contents of the instruction address counter.

If necessary the natural order of following instructions in the program can be disrupted by using control instructions. These instructions include unconditional control transfer instructions (unconditional transfer), in the address part of which is indicated the address of the instruction fulfilled immediately after a given instruction, and also conditional control transfer instructions (conditional transfer) in which transfer addresses are selected according to the feature of the condition determined in previous calculations. Conditional transfer instructions are used extensively when programming branched processes.

The program is control information that provides solution of the problem written in machine codes. The computer control device is designed to decode these codes and to convert them to control signals. Let us consider the designation of the basic assemblies of the control device and their functional relationships during implementation of a single instruction (Figure 5.2).

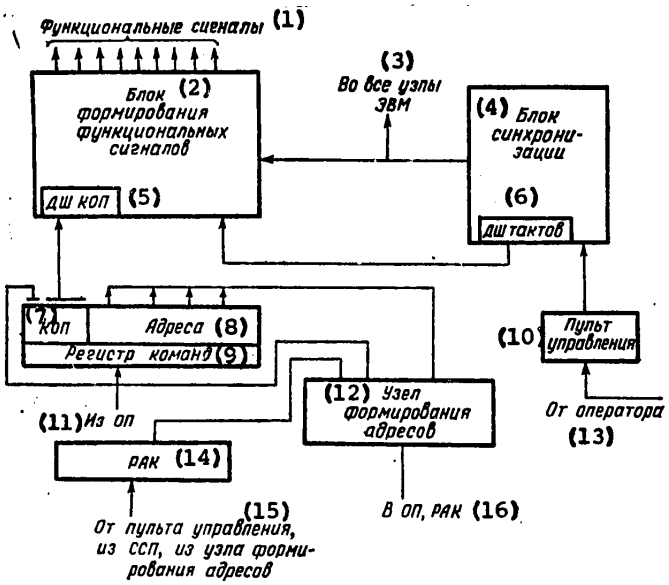

Figure 5.2. Diagram of Relationships of Basic Functional Assemblies of Control Device

[Key on following page]

[Key continued from preceding page]

1. Functional signals
2. Functional signal shaping unit
3. To all computer assemblies
4. Synchronization unit
5. Operational code decoder
6. Time decoder
7. Operational code
8. Addresses
9. Instruction register
10. Control console
11. From internal storage
12. Address shaping assembly
13. From operator
14. Instruction address register
15. From control console, from main internal storage and from address shaping assembly
16. To internal storage and instruction address register

Fulfillment of the program begins after the address of the first program instruction appears in the instruction address register (RAK). The information encoded in the instruction is converted in the control device. The operational part of the instruction is fed to the functional signal shaping unit, where it is converted to control signals which are emitted to all computer assemblies participating in fulfillment of this operation. The address part of the instruction is transferred to the address shaping assembly, from which the effective operand addresses are transmitted to the memory. The operands selected from the internal storage by these addresses are retransmitted to the arithmetic-logic device, where the result remains after the given operation has been performed. Completing the operation, the control device generates control signals that ensure that the result will be sent to the memory according to the address which is also formed in the address forming assembly. The control device forms the address of the next instruction simultaneously with performing the current operation.

Upon completion of the described operations that ensure performance of a single operation, the control device selects the next instruction from the internal storage to the instruction register.

Thus, the control device should perform the following functions:

selection and storage of the instruction during the entire time of fulfilling it;

conversion of the instruction code to control signals;

conversion of the address part of the instruction to find the effective addresses of the operands by which they are selected from the internal storage;

ensure input of data and output of results through the external devices;

provide starting and stopping of the machine;

provide synchronous operation of all machine assemblies when performing different operations.

All the enumerated functions are performed directly in the central control device (TsUU). The basic units of the central control device required to realize

automatic fulfillment of the program--the synchronization unit (BS), instruction control unit (BUK), operations control unit (BUO), interrupt unit (BP) and control console (PU)--are presented in Figure 5.3.

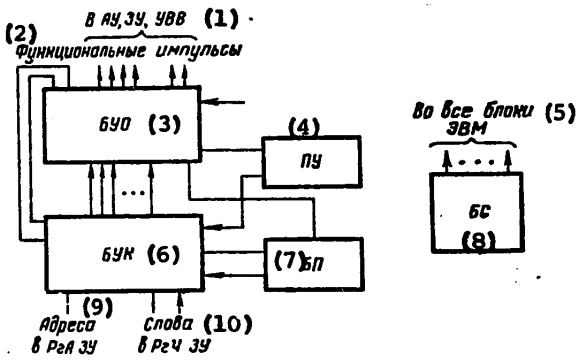

Figure 5.3. Block Diagram of Central Control Device

Key:
1. To address device, internal storage and input-output device
2. Functional pulses
3. Operations control unit
4. Control console
5. To all computer units
6. Instruction control unit
7. Interrupt unit
8. Synchronization unit
9. Addresses in internal storage address register
10. Words in internal storage number register

The synchronization unit (BS) coordinates the operation of all units of the processor in time. The time during which a single instruction is fulfilled from selection from the internal storage to finding the result is called the operating cycle of the control device, which usually corresponds to the operating cycle of the entire machine. The operating cycle of the control device consists of the time intervals during which individual microoperations are performed. This time interval is called the machine cycle. For example, an operand can be read from the internal storage, the contents of the register can be reset or shifted by one digit and so on during one machine cycle. The length of the machine cycle is controlled by the synchronizing pulse generator. The synchronizing pulses are generated continuously by the generator and are fed to the cycle counter, the output code of which is fed to the cycle decoder input. The number of decoder outputs corresponds to the number of cycles comprising the machine operating cycle. The shaping circuit of cycle signals should generate the entire sequence of cycles that ensure realization of a single instruction within one operating cycle (Figure 5.4).

Several microoperations, for which several functional pulses must be generated, can be performed during a single cycle in the processor. The microoperations

realized during a single cycle are frequently interrelated; therefore, these functional pulses should also be separated in time and should be generated in a specific sequence. This leads to the fact that a series of auxiliary pulses are shaped in the synchronization unit, besides the basic series of synchronizing pulses generated by the generator.

Thus, for example, the synchronization unit in the YeS-1020 computer shapes five series of synchronizing pulses: initial synchronizing pulses of series S, main synchronizing pulses of series GI and operating synchronizing pulses of series TI, KhI and SI. In this case each series consists of four pulses which are numbered from the first to the fourth (for example, GI1, GI2, GI3 and GI4).

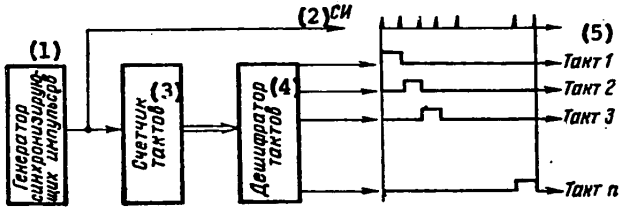

Figure 5.4. Cycle Signal Shaping Diagram

Key:
1. Synchronizing pulse generator
2. Synchronizing pulses
3. Cycle counter
4. Cycle decoder
5. Cycle

Synchronizing pulses of series C are generated continuously in the generator circuits and are used to shape the main and working synchronizing pulses. Time shift of the pulses of the series is provided with respect to each other by a delay line with one input and three outputs (Figure 5.5).

The cycle pulses TI are used to fulfill microinstructions, no-load pulses KhI are used to change the sequence of selecting microoperations and selector pulses SI are used to organize access of the selector channel to the internal storage. As follows from the foregoing, the series of synchronizing pulses have different functional designation but due to the fact that they are all generated on the basis of pulses from the synchronizing generator, the operation of all the assemblies and units in the computer is coordinated when performing any operations provided by the instruction system.

Cycle pulses are generated only when a machine instruction is fulfilled; shaping of the pulses stops upon completion of the program. This is provided by the machine start-stop unit in which disconnection of the synchronizing pulse generator from the time signal shaping circuits is provided.

The operations control unit (BUO) is designed to convert the operational machine code to a sequence of functional pulses that realize this operation in the

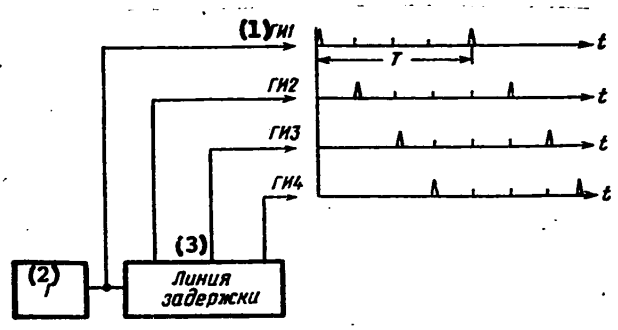

Figure 5.5. Diagram of Generating Series of Synchronizing Pulses

Key:
1. Main synchronizing pulses
2. Generator
3. Delay line

processor. Functional signals in the form of current pulses (functional pulses) are fed from the BUO to those computer assemblies where the operation should be carried out. The input information for this unit is the operational code, which is fed as part of the entire instruction from the internal storage to the instruction register at the beginning of the cycle of fulfilling the instruction (see Figure 5.2).

The method of shaping functional signals in the central control device determines the operating principle of the control device. Two control principles--microprogram and network--are used in the computer.

With the network principle of control, the sequence of functional pulses is controlled by logic circuits. The set of logic circuits provides generation of the control signals which permit any operation presented to the computer to be realized. The set of logic circuits and their relationships in the computer are constant; therefore this control principle is also called the "rigid" logic principle. Any changes in the instruction system or in the algorithms of fulfilling them in machines that utilize this control principle cannot be made without physical changes in the equipment.

The microprogram principle of control, based on replacement of the control logic circuits by a special program stored in the read-only memory, which is frequently called the control memory, is more flexible and convenient to introduce changes into the control system. This memory stores the control signals in the form of microinstructions which are combined into microprograms. A single microprogram is equivalent to a single machine instruction. The microprogram principle of control simplifies the development of computer logic and permits changes of it during development.

Microprogramming permits processors to be developed with a wide set of instructions since an increase of their number requires only that the read-only memory capacity be expanded.

Microprogramming permits one to supplement rather simply the instruction system of a universal computer with a set of additional instructions oriented towards specialized problems and also permits one to give emulative properties to the control system, i.e., it permits a given computer to fulfill programs compiled for other machines. To do this, an additional set of microinstructions that fulfill operations not provided for in the instruction system of a given computer is entered in the read-only memory. The microprogram and network principles of control are considered in more detail in 5.3.

The instruction control unit (BUK) provides for processing of the address part of the instruction, generates the address of the next instruction and switches on the instruction register, instruction address counter, instruction address register and adder for forming the access addresses to the internal storage. The registers, counters and adders of the instruction control unit are program-accessible in models of YeS computers, which means that their contents can be changed by the action of control or operating programs. Together with the interrupt unit (BP), the BUK converts from execution of one program to another during operation of the machine in the multiprogram mode.

The composition of the instruction control unit depends on the characteristics of a specific computer and its designation (the address capacity of the machine, the operand addressing system and so on).

One can use one-, two- and three-address instructions in the computer, which is reflected directly in the time of fulfilling a single instruction and the sequence of processing its address part.

Relative addressing of operands used in the computer is very convenient to the programmer, who does not require data on the internal storage reserves when compiling programs and who can begin recording the instructions from the zero address. But the structure of the instruction control units in which the forming assemblies of effective operand addresses (or access addresses to the internal storage) must be provided, is complicated. Thus,

$$A_{\text{исп}} = A_{\text{отн}} + A_{\text{баз}},$$

where A_{isp} is the effective operand address, A_{otn} is the relative operand address and A_{baz} is the basic address.

Let us consider the operation of the instruction control unit of the example of fulfilling a two-address instruction, which is used most extensively in machines. The two-address instruction has the following structure:

КОП	B1	A1	B2	A2

where KOP is the operating code, B1 is the number of the register in which is located the basic address of the file where the first operand is located, A1 is the relative address of the first operand, B2 is the number of the register in which is located the basic address of the file where the second operand is located and A2 is the relative address of the second operand.

The address of the first program instruction by which the instruction is generated from the internal storage and is transferred through the code buses to the instruction register where it is stored during the entire cycle, is entered in the instruction address register (RAK) prior to the beginning of fulfilling the program. The instruction register consists of several functionally independent parts: an operational code register (RKO;), base number registers (RNB) and relative address registers (RA). The effective addresses are formed in the address adder (SMA), which is one of the main assemblies of the address forming device (Figure 5.6). The address code of the first operand from RA1 and the basic address code from the basic address register whose number is indicated in the RNB are transmitted to the adder. The address found in the adder is transmitted to the address register of the internal storage for reading of the first operand from it. The effective address of the second operand is then formed in a similar manner and is read from the internal storage, after which both operands are retransmitted from the internal storage to the arithmetic-logic device in which the operation is fulfilled and the result is found. The result of the operation can be left in the adder or transferred to the internal storage depending on the modification of the operation to be performed. If the result should be entered in the internal storage, it is recorded in place of the second operand.

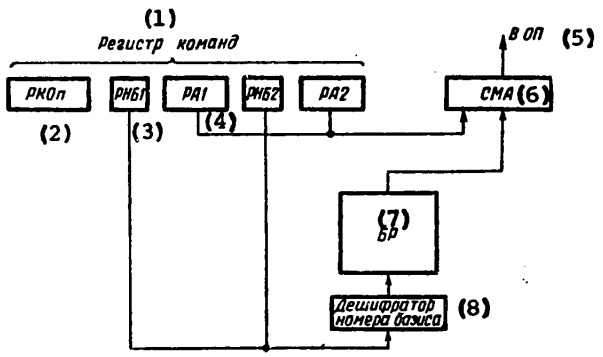

Figure 5.6. Diagram of Effective Address Formation

Key:
1. Instruction register
2. Operational code register
3. Base number register
4. Relative address register
5. To internal storage
6. Address adder
7. Base register
8. Base number decoder

Special instructions in which the address part, besides the basic and relative addresses of the operand, also contains readdressing constants, are used to fulfill cyclic programs in computers. Like basic addresses, readdressing constants are controlled in the address part of the instruction in implicit form--by the number of the index register. In these cases the effective address of the operand is formed in two cycles: the relative and basic addresses are added during the first cycle (the base cycle) and the readdressing constant selected from the index register is added to the contents of the address adder during the second cycle (the indexing cycle).

Assemblies and communication circuits that provide changes in natural following of instructions in programs are provided in the instruction control unit. This disruption of the order of fulfilling programs frequently occurs in realizing cyclic programs or branched processes. Similar types of processes are realized in programs when using special control instructions. The distinguishing feature of these instructions is that they contain the instruction address in the address part to which one should convert during the next operating cycle of the machine.

The next instruction address is formed in the instruction control unit after the current operation has been completed. The appearance of a new address in the RAK denotes conversion to fulfillment of a new operation, i.e., to a new operating cycle of the machine.

The interrupt unit (BP) is a compulsory unit of the central control processor of third-generation computer systems and is designed to realize the multiprogram operating mode. The interrupt unit contains electronic assemblies and circuits that are the apparatus part of the overall interrupt system. Problems of program interruption are considered in detail in 5.4.

The structure of the interrupt unit (BP) of a specific machine is determined by the general characteristics of the interrup system and priorities and also by the principle of forming the first instruction address of the interrupting program.

Let us consider the characteristic features of designing a program interrupt unit on the example of the generalized block diagram of an interrupt unit (Figure 5.7).

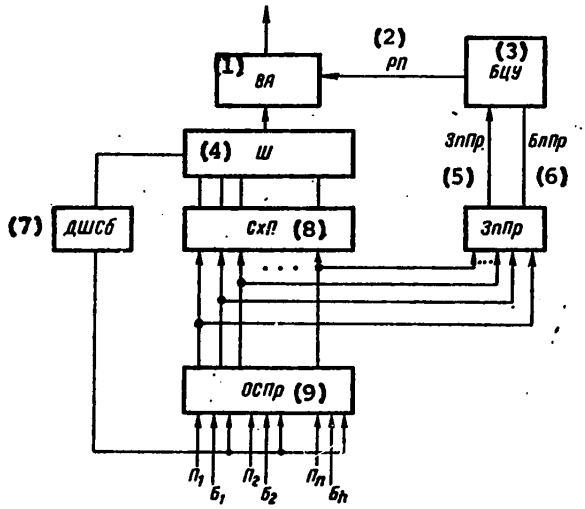

Figure 5.7. Block Diagram of Interrupt Unit

Key:
1. Address generating assembly
2. Transmission authorization
3. Central control device units
4. Encoder

[Key continued on following page]

5. Interrupt request
6. Interrupt unit
7. Interrupt request reset decoder
8. Priority circuit
9. Interrupt signal processing

The interrupt unit includes the following assemblies: interrupt signal processing (OSPr), interrupt request formation (ZpPr), priority circuits (Skhp), interrupt program address coder (Sh) and interrupt request reset decoder (DShSb).

Requests to interrupt (P_1,..., P_n) of a program being executed are fed from different interrupt sources to the circuits of the OSPr assembly and interrupt interlocking signals (B_1, ..., B_n) are fed to these circuits. Only those interruptions which have not been blocked to the program being executed are fed to the output of the interrupt signal processing circuit. Signals are fed from the OSPr output through the interrupt request forming assembly ZpPr to the units of the central control device (BTsU) to change the order of executing the program. At the same time the interrupt request signals are fed from the output of the OSPr to the priority circuit, where the priority of performing the interruptions is determined according to their priorities. Output signals are fed from the priority circuits to the encoder in which the access address to the interrupting program is formed according to the request. This address is fed to the address generation assembly (VA), from which it is retransmitted upon a transfer authorization signal (RP) to the address register of the internal storage. The feature of receiving the corresponding interrupt signal is fed from the coder after access to the n-th interrupting program and a signal to extinguish the n-th interrupt signal at the OSPr output is issued through the reset decoder.

The control console provides operator communications with the machine and permits him to interfere in the calculating process. The console contains devices that indicate the state of the basic assemblies of the processor and permits monitoring of the operation of the processor units. The console contains front control and display panels and an internal panel.

The manual control working members that permit the operator to set the required operating mode of the calculating system--continuous operating mode, single instruction execution mode, repeat execution of instruction sequence mode and so on--are located on the front control panel. The effective address of any cell of the internal storage can be set and access to it can be gained and the number code which will be entered in this memory cell can also be composed by using the switches of the front panel. The address of the external device from which the program should be initially loaded can be assembled on the front panel by means of special switches. The special switches provide setting of modes that perform preventive maintenance and checking operations of the processor.

Indicators of the state of channels, some registers of the processor, the register of state of the program and some synchronization units are located on the front display panel.

The internal panel of the control console contains switches designed mainly for reconfiguration and determination of the internal storage addresses and also switches that control the organization of timer operation.

5.3. Microprogram and Network Principles of Computer Control

The microprogram principle of control has achieved wide distribution in design of computer systems. But the time of performing operations with this principle of control is increased considerably due to the multiple access to the PZU for reading microinstructions that comprise the microprogram. Therefore, highly productive computer systems are constructed by using control devices with "rigid" logic and the microprogram principle of control is used in low- and medium-productive machines.

Younger models of the YeS computers--the YeS-1010, YeS-1020, YeS-1030 and YeS-1040 --have microprogram control devices while older models--the YeS-1050 and YeS-1060 --were developed using the "rigid" logic control principle.

Let us consider in more detail the network realization of the microprogram principle and the "rigid" logic principle.

The Microprogram Principle of Control

As was already pointed out, the microprogram principle of control is based on replacement of the control logic circuits by special microinstructions which are stored in the read-only memory (PT) (Figure 5.8).

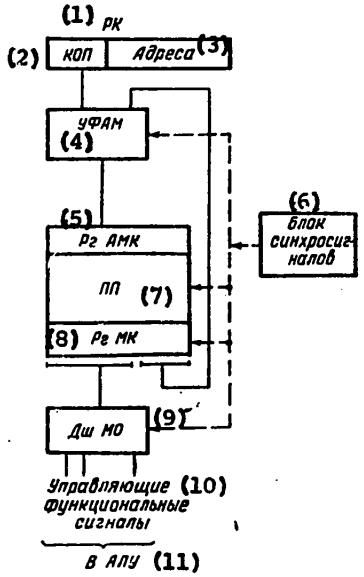

Figure 5.8. Structure of Microprogram Control Device

Key:
1. Instruction register
2. Operating code
3. Addresses
4. Microinstruction address forming assembly

[Key continued on following page]

[Key continued from preceding page]:

5. Microinstruction address register
6. Synchronizing signal unit
7. Read-only memory
8. Microinstruction register
9. Microoperation decoder
10. Functional control signals
11. To arithmetic-logic device

Control signals are stored in the read-only memory in the form of microinstructions. The microinstruction contains information about the microoperation performed during a single machine cycle and also information about forming the next microinstruction address.

Microoperation is an elementary operation performed under the control of a single functional signal (for example, register reset to zero state, shift of register contents by one digit and so on).

The group of microinstructions that realize a single machine instruction or an individual procedure is called the microprogram. The microprogram controls the operation of the machine during one cycle. A single instruction is fulfilled in the YeS computer in two cycles: the instruction selection cycle and the fulfillment cycle. The SELECTION microprogram common to all instructions controls the machine instruction selection cycle. The fulfillment cycle is realized for each specific instruction by its own microprogram. There are two methods of encoding control signals in microprogramming. In the first method one binary digit with a constant number is set into agreement to each control signal in the microinstruction.

The single state of the microinstruction digit means that the control signal should be generated while fulfilling a given microinstruction. The digit capacity of the microinstruction should correspond in this case to the number of microoperations performed by the machine.

A microinstruction can contain ones in several digits, which permits simultaneous fulfillment of several microoperations. But in this case the microoperations to be performed should be compatible, i.e., they should not exclude each other. The simplicity of shaping functional pulses and the capability of time integration of several microoperations are an undoubted advantage of the given method of encoding microoperations.

However, the number of functional pulses in processors of YeS computers may reach several hundreds, which requires a corresponding number of positions to arrange the microinstruction. No more than 10 microoperations can be combined in a single microinstruction; therefore, the microinstruction contains zeros in most positions. This disadvantage leads to inefficient utilization of the storage capacity designed to store microinstructions.

The second principle of encoding microoperations--vertical microprogramming--has found greater distribution. The microinstruction is set into agreement to each microoperation with this method of control. A total of n binary digits of the microinstruction, i.e., the microoperations field, is allocated to the microoperation; a total of 2^n microoperations can be used in the machine.

This method of encoding microoperations is analogous to the method of encoding operations with the only difference that a more elementary operation is performed here, i.e., a microoperation.

Besides the microoperations field, the microinstruction contains other fields, specifically the address assignment field of the next microinstruction since the compulsory method of microinstruction selection is used in the microprograms. This procedure of following microinstructions is determined with the microprogram method of control to save read-only memory cells: many microprograms contain identical microinstructions (such as, for example, register reset, adder reset and so on); therefore, it is feasible to enter these microinstructions only once into the read-only memory and to organize access to them from different microprograms.

The generalized structure of a microinstruction for vertical microprogramming is presented in Figure 5.9. The microinstruction consists of two parts: the microoperations code and the address part. The microoperations code includes data on the microoperation which should be performed and also data on the operand addresses on which this microoperation will be performed. Constants for forming the address of the next microinstruction are indicated in the address part of the microinstruction. The features which appear as a result of performing the current microoperation are taken into account when forming the address.

The structure of a typical microprogram control device is presented in Figure 5.8.

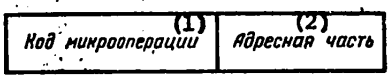

Figure 5.9. Structure of Microinstruction

Key:
1. Microoperations code
2. Address part

The microinstructions are stored in the read-only memory, from which they are selected by addresses formed in the microinstruction address forming assembly (UFAM). The initial address of the microprogram is controlled by the operations code which is fed to the UFAM. The addresses of the next microinstructions are formed from the address constants selected from the address part of the current microinstruction and the features of the result of the current microinstruction. The address formed in the UFAM is fed to the microinstruction address register (RgAMK). The microinstruction read from the read-only memory is entered in the microinstruction register (RgMK), from which the microoperations code is transmitted to the microoperations decoder (DShMO), while the address constants are transmitted to the UFAM. The functional control signals are fed from the output of the DShMO either to the processor units or to other devices, as a result of which the current microinstruction should be realized.

The Network Principle of Control

The main assemblies of the operations control unit in machines that utilize the network principle of control are the operations decoder, functional signal generation assembly and functional signal shaper assembly (Figure 5.10).

The operations decoder converts the machine operations code to a single operations index pulse. The decoder should have a number of outputs equal to the number of operations provided by the instruction system of the given machine. The operations code is fed to the decoder input from the instruction register, to which it is transmitted as part of the instruction from the internal storage at the beginning of the cycle of fulfilling it.

The functional signal generation assembly is a combination of logic circuits that provide shaping of the functional pulses required to realize all the instructions provided for a given computer. Any operation should be fulfilled with a complete set of functional pulses required to fulfill it. As an example let us consider performance of the simplest arithmetic operation in a two-address machine. The instruction fulfillment cycle consists of the following seven time steps for microoperations:

1--ALU adder reset;

2--receiving the effective address of the first operand;

3--transmitting the first operand from the internal storage to the arithmetic-logic device;

4--receiving the effective address of the second operand;

5--transmitting the second operand from the OP to the ALU;

6--performing operations on the operands in the ALU;

7--transmitting the result from the ALU to the OP.

A control pulse is required to perform each of the enumerated microoperations, for which its own logic circuit is provided in the functional signal shaping assembly. The operations index and time pulse should be fed to the inputs of this circuit. The time pulses fed to the inputs of the logic circuits provide the time relations of following the functional pulses (Figure 5.11). The indices of different operations can be fed to the same input of any logic circuit if these operations require the compulsory presence of a given functional signal for fulfillment. Thus, for example, functional pulses that form the effective addresses are required to perform all arithmetic operations.

In some cases the sequence of control signals may depend on some additional features. For example, the operand may be transmitted from the memory to the arithmetic-logic devices in direct or reciprocal code depending on its sign. In this case an additional index signal is fed to the input of the logic circuit (Figure 5.12).

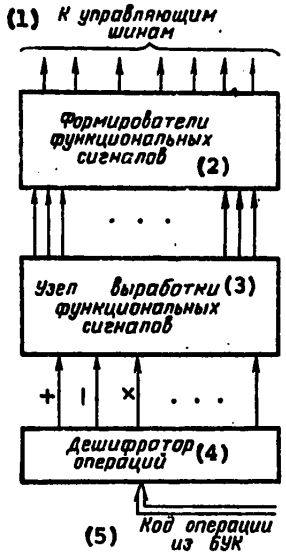

Figure 5.10. Basic Assemblies of Control Device with "Rigid" Logic

Key:
1. To control buses
2. Functional signal shapers
3. Functional signal generation assembly
4. Operations decoder
5. Operations code from BUK

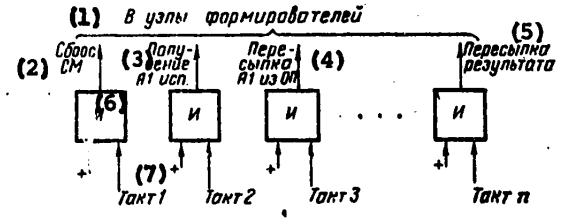

Figure 5.11. Assembly of Logic Circuits that Provide Time Relations of Following Functional Signals

Key:
1. To shaper assemblies
2. Adder reset
3. Reception of effective A1
4. Transmission of A1 from internal storage
5. Transmission of result
6. Impulse
7. Cycle

Thus, there is a set of control pulses at the output of the signal functional shaping assembly that are called on to perform the operation whose cose is fed to the decoder input during this operating cycle of the machine.

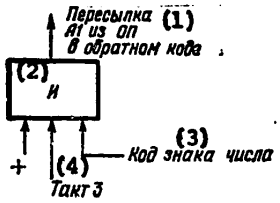

Figure 5.12. Diagram of Generating Functional Signal According to Additional Features

Key:
1. Transmission of Al from internal storage in reciprocal code
2. Impulse
3. Number sign code
4. Cycle

The shaper assembly generates control pulses of the required amplitude, length and steepness of the fronts.

5.4. The Multiprogram Operating Mode and Interrupt System

Problems can be solved in the unified computer system in single- or multiprogram modes. In the single-program mode the computer solves only one problem and converts to the next problem only after the previous one is finished. In this case only one program to be fulfilled is located in the internal storage in each moment of time.

In the multiprogram mode the machine can perform several tasks. In this case several programs to be fulfilled simultaneously, the memory resources between which are distributed by the operating system, are stored in the internal storage.

The advantage of multiprogram computers, to which the computers of the unified system are related, is the capability of organizing different operating modes to service user programs, for example, batch processing , time-sharing, interrogation-answer and so on.

In the multiprogram mode, the processor fulfills instructions of only one program at each moment of time from all the programs in the internal storage. Conversion from fulfilling one program to another occurs when it is more feasible to fulfill a new program than to continue the previous one. For example, when fulfilling some program, it became necessary to exchange data with external devices or to convert from an operating program to a service, control or other program.

Conversion from fulfilling a sequence of instructions of a single program to a sequence of another program is called interruption in the multiprogramming mode.

The SSP has the format of a binary word 64 bits long. Its structure is presented in Figure 5.13.

Let us consider the designation of individual SSP fields.

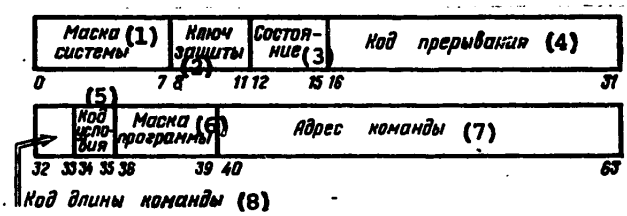

Figure 5.13. Structure of Program Status Word (SSP)

Key:

1. System mask
2. Protection key
3. State
4. Interrupt code
5. Condition code
6. Program mask
7. Instruction address
8. Instruction length code

The SYSTEM MASK field includes eight bits (0-7): 0 is the multiplex channel mask, 1-6 is the selector channel mask and 7 is the signal mask of external interruptions. This field is connected in the SSP to external signals (including signals from the "INTERRUPT" button on the control console). Eight bits of the system maks are used selectively or all together to mask external interruptions and input-output interruptions. External signals and channels (multiplex and selector) are masked when the corresponding bit of the system mask is set to the zero state. An interruption occurring for any reason is stopped in this case. If the bit of the mask corresponding to this interruption is in the one state, the interruption is authorized.

The need to mask interruptions is caused by the fact that situations may occur during operation of the machine when two requests for interruption appear simultaneously. To avoid this, interruption masking is entered, i.e., interruption, but with storage, is prevented.

The SSP contains masks for different types of interruptions: a system mask, verification circuit mask and program mask, each of which masks a specific type of interruption.

The PROTECTION KEY field includes 8-11 bits and is used to arrange the program protection key. For purposes of protection, the memory is divided into units, to each of which a protection key four bits long is assigned. This same key has a program that occupies these memory units. Program protection keys are selected from SSP with each access to the memory and is compared to the memory protection key. Nonconformity of these keys is regarded as violation of memory protection and causes a prohibition of access and interruption of the program.

The STATUS fields contains 12-15 bits and reflects the status and operating modes of the machine. Bit 12 characteristizes the operating mode with KOI-8 code (if the value of the bit is equal to 1) or with DKOI code (if the value of the bit is equal to 0).

Organization of the interrupt system. The interrupt process is accomplished in the unified computer system both by hardware and software. A given sequence of instruction processing may be disrupted by interruption of the calculating process.

All possible interruptions in the YeS computers can be divided into five groups:

due to machine verification circuits (machine interruptions);

by program errors (program interruptions);

upon access to the SUPERVISOR (SUPERVISOR call);

by signals from external sources (external interruptions);

due to input-output devices (input-output interruptions).

Let us consider the nature and causes for each group of interruptions.

1. Machine interruptions occur when breakdowns are detected during fulfillment of the program. The causes of machine interruptions may be errors in the evenness of a machine word or address upon access to the internal storage, malfunctions in the operation of a channel or external device, malfunctions of the power supply system and so on.

Processing these interruptions depends on the error recording programs located in the operating system. There are several types of error recording programs, each of which signals the state of the processor and channels to the operator with different degree of detail. Depending on the nature of the error or malfunction, these programs either convert the processor to the standby state or transfer control to the CONTROLLER program to continue fulfilling the program to be processed.

2. Program interruptions occur when unusual situations arising during fulfillment of the program appear. The reasons for these situations may be errors in the operations code, incorrect addressing, overflow of the digit matrix and so on.

A total of 15 different types of program interruptions, to each of which corresponds its own interrupt code, is provided for in all models of the YeS computers. The program interruptions are enumerated below:

1) incorrectness of operations code (the operations code is not indicated or the operation is not contained in the given model of the processor);

2) a privileged operation (incorrect utilization of an operation. If it is encountered in the PROBLEM state, then an interruption occurs);

3) incorrection of EXECUTE instruction (if the EXECUTE instruction is transmitted to a different instruction of the same type);

4) violation of memory security (the key of the memory unit for the instruction or operand does not coincide with the protection key in the program status word);

5) incorrect addressing (if the address indicates any part of data, instruction or control word and goes beyond the limits of the memory of a given machine);

6) incorrect specification (data, instruction or control word address does not correspond to the integer boundary of the given information unit; the register address with floating point differing from 0, 2, 4 or 6 is indicated; the length of the multiplier or divisor in decimal arithmetic operations exceeds the permissible length--15 numbers and 1 sign; the field of the first operand is shorter or equal to the field of the second operand during decimal multiplication or division; not all address bits of the memory unit are equal to zero in the SET MEMORY KEY or READ MEMORY KEY instructions of the four least significant bits);

7) incorrect decimal data (if an incorrect number or character code is detected in operations of decimal arithmetic, editing or conversion to binary system; the fields overlap incorrectly in decimal arithmetic operations or the number of most significant zero numbers is less in the multiplicand field than in the multiplier field);

8) overfilling with fixed point (conversion from most significant bits occurs or the most significant bits are lost in addition, subtraction and shift operations or in operations on number signs. In this case the information located outside the register is lost;

9) incorrect division with fixed point (if the quotient during division by zero is not placed in the result register or if the result of the CONVERSION TO BINARY instruction exceeds 31 bits. In this case conversion is stopped but the information located outside the register is lost; division is stopped);

10) decimal overflow (if the result is not placed in the designated field the operation stops, but information that has emerged beyond the field is lost);

11) incorrectness of decimal division (if the quotient exceeds the length of the field indicated for it);

12) exponent overflow (if the result has a characteristic exceeding 127 during addition, subtraction, multiplication or division with floating point; the operation stops in this case;

13) loss of exponent in operations with floating point (if the result has a characteristic less than zero during addition, subtraction, multiplication or division; a zero is recorded instead of the result; the operation is completed);

14) loss of significance (zeros were in all the digits in the mantissa during addition and subtraction in operations with floating point);

15) incorrect division with floating point (if the divisor has zero mantissa).

Operations are stopped during interruptions indicated in items 1-6, 11 and 15. A program interrupt processing subroutine is provided in the OS [operating system] YeS EVM SUPERVISOR. If program interruptions occur, control is transferred to it for emergency completion of the task and corresponding signalling.

3. Interruptions during access to SUPERVISOR are caused by the SUPERVISOR CALL instruction. The main designation of this instruction is to transmit a specific message contained in the form of a code in the instruction to the control program. The given instruction provides for switching of the computer from the PROBLEM state to the SUPERVISOR state.

The SUPERVISOR is the part of the control program that controls the entire calculating process in the machine. It is a set of programs fulfilled in response to requests coming from different sources which are realized through the interrupt system.

4. External interruptions occur in cases when signals appear from the facilities controlled by the machine, from the operator from the control console, when the "INTERRUPT" button is pressed, from the time counter and so on.

5. Interruptions from input-output devices provide the processor with the capability of receiving information about the state of the channels and external devices and to respond to these signals. These interruptions are used to organize parallel operation of the channel processor and external devices. Interruptions are made only after a current instruction is completed by the processor. The resulting interruption permits the SUPERVISOR to determine the state of channels and peripheral devices and to verify that input-output operations have been fulfilled. Since the request for interruption from the input-output device may appear suddenly from several peripheral devices at the same time, priority is established for these cases and only one request is processed.

The INPUT-OUTPUT SUPERVISOR (one of the SUPERVISOR programs) fulfills requests immediately or if several of them come in simultaneously, establishes priority, it takes a request to fulfill and input-output operation out of turn if the given device is ready for operation, it plans fulfillment of programs that process input-output errors and it gives instructions to complete an input-output operation. Interrupt processing is completed by transfer of control to the CONTROLLER.

The program status word (SSP) is intended to control the sequence of instruction selection and also to establish and display the state of the machine with respect to the program being fulfilled at a given moment.

Fulfillment of any program is controlled according to the information contained in the program status word.

The SSP can have three values: "current," "new" and "old."

A word which controls a program being fulfilled at a given moment of time is called a current SSP.

Upon interruption this SSP is stored in the internal storage as an "old" SSP and a "new" SSP, corresponding to the interrupting program, is entered in its place.

An "old" SSP is recorded as a "current" SSP at the end of fulfilling an interrupting program to transfer to an interrupted program. Therefore, two SSP, called "old" and "new," which are located in specific cells of the internal storage, correspond to each group of interruptions.

Bit 13 denotes the interrupt mask from the machine verification circuits. Bit 13 is in the unitary state in which interruptions from the verification circuits are authorized. In this case an external signal is emitted about the malfunction and diagnostic procedures are implemented. If the "VERIFICATION" switch on the control console is set to the on state, the appearance of machine malfunction causes a shutdown. If bit 13 is in the zero state and the switch is off, interruptions during machine malfunctions are blocked. The malfunction signals are not emitted in this case, diagnostic procedures are not carried out and the "ERROR IN MACHINE" condition is retained in anticipation of processing.

Bit 14 reflects the WAIT state. If it is in the zero state, then instructions are selected in the usual sequence when fulfilling the program, i.e., the next instruction whose address is indicated in the SSP instruction address field is selected when the current instruction is completed. In this case the processor is in the COUNTING state. If bit 14 is in the one state, then the next instruction is not selected and fulfilled and the machine is switched to the WAIT state. It will continue until input-output interruption or external interruption, which results in replacement of the "old" SSP by a "new" SSP in which bit 14 is in the zero state.

Bit 15 reflects the PROBLEM or SUPERVISOR state. If bit 15 contains a one, the processor is in the PROBLEM state and the problem program is fulfilled; if the bit contains a zero, the processor is in the SUPERVISOR state and the supervisor program is fulfilled. When fulfilling the problem program, random selection of a privileged instruction causes program interruption. The use of all instructions, including privileged instructions, is permitted in the SUPERVISOR state.

The INTERRUPT CODE field includes bits 16-31, in which the causes of interruptions are recorded.

The INSTRUCTION LENGTH CODE field includes bits 32 and 33 and contains instructions on the length of the last instruction, which was unfulfilled prior to the reason for the interruption.

The CONDITION CODE field contains bits 34 and 35 and reflects the feature of the result after the arithmetic operation has been fulfilled. Four combinations of binary codes--00, 01, 10 and 11--are possible in these bits. These codes correspond to the result features for algebraic addition: 00--zero, 01--less than zero (negative result), 10--greater than zero (positive result) and 11--overflow. The result feature code is set at the end of an addition or subtraction operation (decimal and binary algebraic addition). This code retains its value in the "current" SSP until completion of the next operation, which may change it.

The condition code also permits one to determine the nature of the result after comparison. Upon completion of the given operation three different comparison codes can be found--00--operands are equal, 01--first operand is less than second and 10--first operand is greater than second operand.

The result feature reflects the status of the processor after completion of a given operation and is used for program control.

The PROGRAM MASK field includes bits 36-39 that contain mask codes for four of 15 program interruptions: bit 36--overflow mask with fixed point, bit 37--decimal overflow mask, bit 38--loss of exponent mask (X > 0) during operations with floating point and bit 39--loss of significance mask (m = 0) with the same operations.

If the corresponding bit is in the unit state, interruptions are authorized and if it is in the zero state, interruptions are blocked.

The INSTRUCTION ADDRESS field (bits 40-63) is used to indicate the instruction address to which one must convert to restore fulfillment of an interrupted program. Since interruption may occur only after completion of an instruction, the address of the next instruction which would be fulfilled if the interruption had not occurred rather than the address of the last fulfilled instruction will be in the INSTRUCTION ADDRESS field of the "old" SSP. The contents of the INSTRUCTION ADDRESS field of the "old" SSP should be replaced by the SUPERVISOR to find the address of the last completed instruction. To do this, the SUPERVISOR utilizes data in bits 32 and 33 of the SSP on the length of the last instruction to which one must return after processing the interruptions.

Interrupt processing. The factors that cause interruptions of each of the groups enumerated above are processed by a separate program, which is part of the SUPERVISOR, i.e., five interrupt groups correspond to five SUPERVISOR programs. All the enumerated interruptions include the following sequence of operations: stopping of the program being fulfilled and transfer of control to the interrupting program, storage of the status of the interrupted program so as to return to continuation of it after processing of the interruption, fulfilling the interrupting program and transfer of control to the interrupted program and restoring the information of the interrupted program and restoring fulfillment of it.

The interrupt procedure for all five groups of interruptions includes storage of the "current" SSP in the cell designated for the "old" SSP and in selection of a new SSP from the corresponding cell which becomes the "current" SSP. The "new" SSP, having become the "current" SSP, controls fulfillment of the interrupt program (Figure 5.14). The last instruction in the interrupt processing program is the LOAD SSP instruction, by which the "old" SSP is selected in place of the "current" SSP and the machine returns to fulfillment of the interrupted program.

Processor states. The processors of the Unified Computer System may be at each moment of time in states determined by pairs of mutually exclusive program states of four types:

STOP-OPERATION;

WAIT-COUNTING;

SUPERVISOR-PROBLEM;

INTERRUPTION MASKED--INTERRUPTION AUTHORIZED.

Changing from one state to another is usually accompanied by interruption of the program after the instruction has been completed and by variation of the SSP.

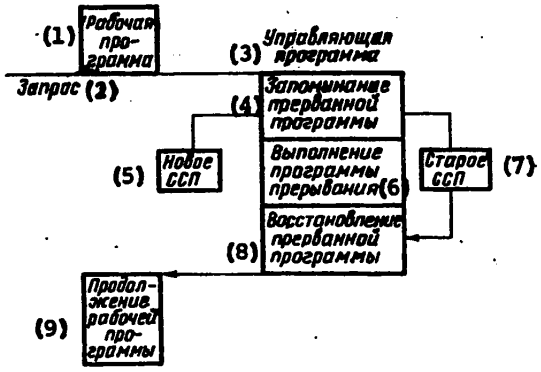

Figure 5.14. Diagram of Interrupt Processing Sequence

Key:

1. Operating program
2. Inquiry
3. Control program
4. Storage of interrupted program
5. New SSP
6. Fulfillment of interrupt program
7. Old SSP
8. Restoration of interrupted program
9. Continuation of operating program

The first pair of STOP-OPERATION states is not reflected in the SSP. Switches between these states are achieved by pressing the corresponding keys on the control console. The STOP state is characterized by the fact that instructions are not fulfilled while requests for interruptions are disregarded. Changing to this state is achieved by pressing the "STOP," "POWER SUPPLY ON" and "EXTINGUISH" keys on the control console.

The processor can fulfill instructions and service interruptions in the OPERATION state. Changing to this state is provided when the "START" keys are pressed and also during initial loading of the program.

The remaining three pairs of states can be assigned only by program--by changing the values of the corresponding SSP digits.

The WAIT state is entered by the program to wait for an interruption, for example, due to input-output. In this state the instructions are not fulfilled but requests for interruptions due to input-output and external interruptions are received and processed.

The "COUNTING" state denotes fulfillment of the usual sequence of selection and fulfillment of program instructions. Code 1 in bit 14 on the SSP corresponds to the "WAIT" state and code 0 in this bit corresponds to the COUNTING state.

Fulfillment of all instructions, both privileged and unprivileged, is authorized in the SUPERVISOR state. Machine operation is controlled in this state after interruption and conversion from the PROBLEM state.

The problem is solved in the PROBLEM state by means of problem program instructions. All privileged instructions related to input-output and memory protection in this state and also LOAD SSP, SET SYSTEM MASK and DIAGNOSIS instructions are impermissible. Code 0 in bit 15 of the SSP corresponds to the SUPERVISOR state, while code 1 in this same bit corresponds to the PROBLEM state.

The fourth pair of interruptions--INTERRUPTION MASK-INTERRUPTION AUTHORIZED--reflects the processor's response to external interruptions and also to interruptions from the machine monitoring circuits, from input-output and some program interrupinterruptions.

If the processor is in the INTERRUPTION AUTHORIZED state, then the authorized interruptions are realized by the processor. In the INTERRUPTION MASKED state, input-output interruptions, external interruptions and interruptions from the machine monitoring circuits wait for processing while program interruptions are disregarded.

The processor is switched to the corresponding state by changing the value of the mask bit in the SSP.

An interruption is assumed to be masked (prohibited) if a zero is contained in the corresponding bit of the SSP. If there is a one in this bit, interruption is authorized. Interruption priorities are used when several interruptions occurred simultaneously. The depth of interruptions has four priorities for groups of interruption sources. Interruptions from machine monitoring circuits have the highest priority. Fulfillment of the current instruction is stopped when they occur. Interruptions from input-output devices, external and program interruptions then proceed in the order of priority and program interruptions and interruptions due to access to the SUPERVISOR have identical priority since they mutually exclude each other.

If requests for program and external interruptions and input-output interruptions occur simultaneously, the machine responds to these interruptions in the following manner. The "current" SSP, i.e., the SSP for the interrupted operating program, is stored in cell 40 (YeS-1020 and YeS-1030) of the main memory, while the "new" SSP is loaded in place of the "current" SSP from cell 104. The "current" SSP, having become the "new" SSP of program interruptions, is stored in cell 24, while the "new" SSP from cell 88--the external interruptions SSP--is loaded in its place. After this the "new" SSP is stored in cell 56 and the "new" SSP selected from cell 120--the input-output interruptions SSP--becomes the "current" SSP.

Interruptions are realized in the order of their priority or significance. In the considered case, since the input-output interruptions SSP became the "current" SSP, it is realized first.

5.5. Designation and Composition of Arithmetic-Logic Device

The arithmetic-logic device (ALU) is used to process operands according to given algorithms. Operands are machine words of fixed or variable length. Operands can be binary integers or fractions represented in a form with fixed and floating point, decimal integers, logic codes and alphanumeric codes.

The ALU performs arithmetic operations, logic operations and also address arithmetic operations (address modification). The algorithms of the operations enumerated above include a definite sequence of elementary operations (microoperations):

reception of operand code;

conversion of operand code;

adding of codes of two operands;

shift of operand code;

output of result code.

The following assemblies are provided in the ALU to perform these operations:

registers--to store the operand codes for the time of performing operations on them;

shifters--to shift to code by one or several digits to the right or left;

number code converters--to convert a direct code to a reciprocal or supplementary code;

adder--to perform operations on operands.

A number of factors such as the type of operands to be processed in the ALU, organization of performing operations on operands and methods of communication between basic assemblies of the ALU is taken into account when forming the structures of ALU in computers. The following types of ALU can be distinguished.

Depending on the number system being used, ALU are divided into ALU for processing binary numbers and ALU for processing decimal numbers. The latter provide a significant time advantage since no time need be lost on preliminary conversion of numbers from the decimal to the binary number system. At the same time the algorithms for performing the operations on numbers represented in the decimal number system are much more complex than the algorithms for operations on binary numbers and realization of them requires that the ALU apparatus be more complicated. Therefore, ALU for processing decimal numbers are used only in those cases when large decimal information files for simple calculations must be processed.

ALU are divided into those for processing numbers with fixed point and those for processing numbers with floating point according to the method of number representation.

ALU for processing numbers represented in a form with floating point have a more complex structure and require a more complex algorithm for realization of operations, since, along with performing operations on the mantissas of numbers, the orders of numbers participating in the operation must be processed.

ALU can be divided into unit and multifunctional according to the nature of utilizing the components and assemblies.

In multifunctional ALU, operations for all forms of representation of numerical information are performed by the same circuits which are switched as a function of the required operating mode.

In unit ALU, its own function is attached to each unit: processing of binary numbers with fixed point, processing of binary numbers with floating point, processing of decimal numbers and so on.

Multifunctional ALU are used in low- and medium-productive machines. The use of a universal adder that performs all operations permits the volume of ALU equipment and its cost to be reduced. Unit type ALU are used in high-productive computers. Their use increases the speed of calculations since the different units can perform operations in parallel on information of various types, but the expenditures for equipment increase considerably in these ALU.

ALU can be divided into parallel and sequential operation types according to the methods of organizing the performance of operations on operands.

An ALU that performs an addition (subtraction) operation on all the digits of numbers simultaneously is called a parallel ALU and has a parallel adder. A sequential ALU has a single-digit adder in which the addition operation is carried out digit by digit. Sequential ALU are used in low-productive computers in which the important factor is the cost of the device.

Medium-productive computers usually have sequential-parallel type ALU and high-productive computers have parallel type ALU.

ALU are divided by the type of communications between basic assemblies into devices with direct communications and with mainline structure. In ALU with direct communications, the adder, control circuits of operations on operands and information transmission control circuits are directly connected to the outputs of the corresponding registers. In this case the operands participating in specific microoperations are read from specific registers and results are formed in specific registers.

In ALU with mainline structure, the circuits for conversion of information are separated into a separate unit while the registers are used only to store operands during their processing. The input and output circuits of the registers therefore contain only information reception and output circuits. The information conversion unit, which includes an adder, shifter and a number of other circuits, is connected to the registers by two mainlines--input and output. A switch that connects any of the registers to the mainline controls the output of information to the output mainline.

ALU with mainline structure are widely used in processors with microprogram control.

An identical set of arithmetic and logic operations, that include operations of binary arithmetic on numbers with fixed and floating point, operations of decimal arithmetic and logic operations, is performed in the ALU of all computers of the unified system.

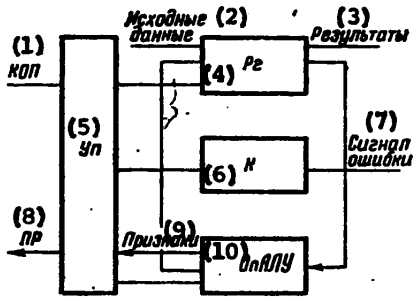

Figure 5.15. Generalized Block Diagram of ALU

Key:

1. Operation code
2. Input data
3. Results
4. Register
5. Control circuit
6. Monitoring circuit
7. Error signal
8. PR
9. Features
10. ALU operation

A generalized block diagram of an ALU (Figure 5.15) for all models of the Unified Computer System includes four basic parts:

register group (RG) designed to receive and arrange operands and results;

operational part (OpALU) in which operands are converted according to algorithms stored in the machine;

monitoring circuits (K) that provide continuous operational monitoring and diagnosis of errors;

control circuits (UP) in which control signals (US) are shaped that coordinate the interaction of all ALU units with each other and with other units of the central processor.

The register unit is connected to the internal storage of the computer and general-purpose registers (RON) of the processor. The number of registers in the unit and their digit capacity are different in different models of YeS EVM. This is determined by the difference in methods of reception, arrangement and operation of data when performing operations.

The information to be converted is analyzed and the feature signals on the basis of which the control circuits form and issue the result feature to the central

processor are formed at different steps of performing the operation for operational control of operation of the unit in the operational part of the ALU.

Conversion to fulfillment of the next instruction is built into the YeS EVM by the asynchronous feature; therefore, the processor emits an end of operation signal (SKOp) to the central processor upon completion of an operation and the ALU converts to performance of the next operation when the beginning of operation signal (SNOp) comes in.

The high-productive YeS-1050 computer has the unit principle of construction of the operational part of the ALU (Figure 5.16). Two units--the arithmetic adder unit (BAS) and the digital decimal arithmetic unit (BATs)--may be distinguished in it.

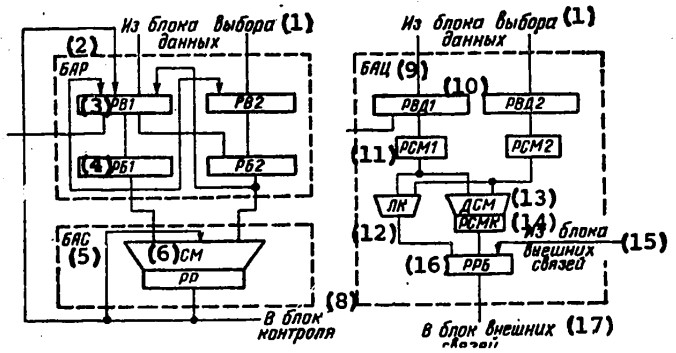

Figure 5.16. Operational Part of ALU of YeS-1050

Key:

1. From data selection unit
2. Arithmetic register unit
3. Input register
4. Buffer register
5. Arithmetic adder unit
6. Adder
7. Result register
8. To monitoring unit
9. Digital decimal arithmetic unit
10. Data input register
11. Adder register
12. Logic switch
13. Decimal adder
14. Adder correction register
15. From external communications unit
16. Byte result register
17. To external communications unit

The arithmetic adder unit (BAS) is designed to perform arithmetic operations in the binary number system and logic operations on operands of fixed formats. Its basis is a 64-digit parallel operation binary adder of combination type. Because of the capability of switching parts of the adder, numbers of different fixed formats with fixed and floating point can be processed in it. Logic operations are performed by the registers of the arithmetic register unit (BAR) and the necessary shifts of operands are made in it by exchange transmissions between input registers RV1 and RV2 and buffer registers RB1 and RB2. The result of the operation is transferred from the result register (RR) to register RV1, which is at the same time the output register of the ALU.

The decimal (digital) arithmetic unit (BATs) is used for byte by byte processing of operands. There is an eight-digit decimal adder (DMS) in the unit for operations on decimal numbers. An eight-digit logic switch (LK) is provided for logic operations on fields of variable length. The input registers of this unit RVD1 and RVD2 have a length of 64 digits and are used to store operands. The necessary bytes, which are transferred through the intermediate single-byte adder registers RSM1 and RSM2 to the decimal adder or logic switch, are selected from the contents of RVD1 and RVD2 during each cycle of performing the operation. The result byte is fed to the result register (RRB). When decimal arithmetic operations are being carried out, each result byte is corrected in the adder correction register (RSMK).

The operational part of the ALU is represented in the YeS-1030 model by a single unit joined to the register unit (Figure 5.17). Its basis is a universal 32-digit adder that performs operations in binary and decimal number systems.

The ALU adder is also used to calculate effective addresses. To do this, the address part is transferred to the adder during the instruction selection cycle while the formed addresses are sent to the address register (RA). Besides the adder, there is a byte logic processing assembly (UOB) in the unit designed for byte by byte logic processing of the operands of fixed and variable formats and the UOB is also used to compare the exponents of operands with floating points.

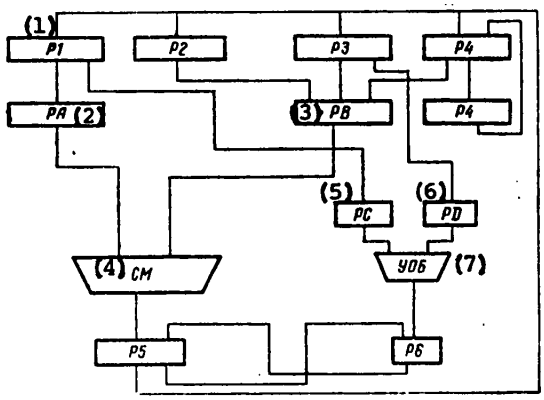

Figure 5.17. Operational Part of ALU of YeS-1030

Key:
1. Register
2. Address register
3. Input register
4. Adder
5. Adder register
6. Data register
7. Byte logic processing assembly

The operational unit communicates with the internal storage through register R5, which performs the functions of input and output registers. The received operands are arranged in registers R1-R4 and the second operand is received in registers R1 and R2 while the first is received in registers R3 and R4. If the operands are 32-digit, they are arranged in registers R1 and R3. Shifts are made in register R4.

Operands (parts of them) are placed in registers RA and RV for addition in a combination type adder. If operands are transferred from registers R1-R4 to registers RA and RV, their codes are converted if necessary. The result is transferred to R5 and the transmission can be direct or with a shift. When performing logic operations, the data bytes are transmitted sequentially to input registers RS and RD. The result bytes are stored in single-byte register R6. The result bytes are transmitted from this register to register R5, being arranged sequentially in it.

The operational part in the ALU of the YeS-1020 (Figure 5.18) is a universal switched arithmetic-logic unit (ALB). Byte by byte processing of all types of data is carried out and effective addresses are formed in it.

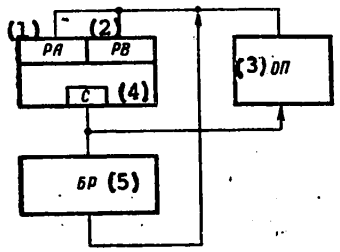

Figure 5.18. Operational Part of ALU of YeS-1020

Key:
1. Address register
2. Input register
3. Internal storage
4. Switch
5. Register unit

All arithmetic and logic operations are realized in the ALB by a switched combination circuit as the aggregate of elementary operations: logic operations, digit adding operations, shift operations and so on. The microprogram control unit of the central processor controls the ALB.

The ALB has two single-byte input registers RA and RB to which the next bytes of the operands to be processed are fed for the time the next microoperation is carried out. Registers of the register unit (BR) of the processor and the information registers of the internal storage (OP) having two-byte structure are used in the YeS-1020 to store the operands and intermediate and final results.

The enumerated registers are connected to the ALB by input and output mainlines eight information bits wide. The information read from the OP is transferred to registers BR through the ALB in the considered communications circuit and the number of the register to which the information is transmitted is controlled by means of switch S, which is controlled by microprogram. Information is issued from the registers to the internal storage in similar fashion.

This structure of the ALB and communications between assemblies was caused by the desire to reduce the volume of processor equipment and to use the same registers and assemblies for different operations.

Chapter 8. Peripheral Devices

8.1. Designation and Classification of Peripheral Devices

A large number of peripheral devices (PU) is used in modern computers.

All peripheral (external) devices can be divided into three basic groups:

input-output devices (UVV);

external storage devices (VZU);

operator-computer communication devices.

Each of the indicated groups of devices is classified by the designation and methods of information input-output.

Input-output devices are used to receive input data and programs and also to read out the results of calculations to machine carriers or for printout. The following are used as input-output devices:

a) information input devices using the keyboard of computer control consoles, teletypes, typewriters, bookkeeping and other keyboard machines;

b) information entry devices from machine carriers (punchcards, papertapes and magnetic tapes);

c) information entry devices from machine-readable documents--automatic reading machines;

d) information output devices to machine carriers;

e) information printout devices;

f) graphic input-output information devices (information display devices--displays and graph plotters.

External storage devices (VZU) are designed for memorizing, storage and readout of large volumes of information. Information is exchanged between external and internal storage devices during computer operation. External storage devices store information on a movable magnetic carrier. Magnetic tapes, drums, disks and cards are used as these carriers.

Operator-computer communication devices are designed for direct exchange of information between man and computer. These devices can be installed in the immediate vicinity of the machine or at user stations separated from the machine by great distances. In the latter cases the devices are installed at user terminals (AP) and are called terminal devices. Operator-computer communication devices include console typewriters, portable consoles with group control device designed to service users separated a considerable distance from the machine and also display devices--displays and display panels.

Due to the presence of standardized communications channels (input-output channels), a large number of peripheral devices can be connected simultaneously to the processor in modern computers.

Input-output channels provide the capability of working with a computer with variable composition of the peripheral devices, which has advantages compared to machines having constant set of peripheral devices, for example, the capability of the user selecting the type of devices available to him and replacement of obsolescent devices with more modern devices.

It is known that information is exchanged between the internal storage and peripheral devices in the input-output organization system of the YeS EVM by using selector (KS) and multiplex (KM) channels. The channels differ from each other by the capability of simultaneous servicing of several peripheral devices.

Control of PU operation is standardized: there is a standard format of instructions, control and information words and information format for control of any peripheral device. This provides the capability of connecting peripheral devices of different types to the channels.

There are control devices for specific PU (peripheral control devices--UVU) for organizing exchange with the peripheral devices.

Communications are accomplished between the input-output channels and the UVU by means of a standardized communications system, which is called a standard input-output interface.

Input-output devices can be connected to the multiplex or selector channel of any model of computer in the YeS EVM by means of the indicated interface. Input-output devices can operate in two modes--multiplex and monopole--when connected to a multiplex channel.

The operating principle of the channels and interface and also organization of information exchange between peripheral devices and the internal storage were considered in detail in Chapter 7.

Let us briefly consider the structure of the input-output system of computers of the Unified System shown in Figure 8.1.

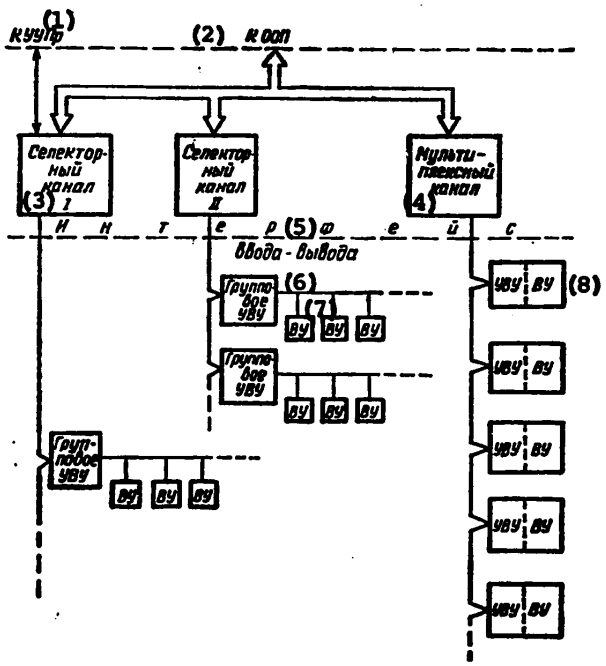

Figure 8.1. Input-Output System of YeS EVM

Key:

1. To control device
2. To basic internal storage
3. Selector channel
4. Multiplex channel
5. Input-output interface
6. Group peripheral control devices
7. Peripheral devices
8. Peripheral control devices

The hardware required to organize exchange with peripheral devices is separated into two levels--lower level, which includes the control device of a specific peripheral device, and upper level, which includes devices that control the operation of all peripheral devices in a system with a processor and basic internal storage. The lower level includes peripheral control devices (UVU). These devices are divided into group and single. Single UVU are used to connect only a single peripheral device to the UVU. A group UVU is designed to service several peripheral devices of the same type. The upper level of the input-output system is an independent functional device--input-output channel, that services the data exchange process between the peripheral device and the basic internal storage under the control of the processor.

Let us note in conclusion that development of peripheral devices with different functional designation in modern computers affects to a greater degree the expansion of the sphere of influence of computers for processing economic information. Besides traditional peripheral devices which are required for machine use independently of the areas of their application (VZU on magnetic carriers, punch card and papertape input-output devices and alphanumeric printers), devices that provide remote information processing (user terminals, different operator consoles with information display on an ELT [cathode-ray tube]--displays and so on) are also used in modern computers.

Auxiliary functional input-output devices contribute to an increase of computer productivity, organization of large-capacity external memory, operator dialogue with the computer and operation of time-sharing and remote data processing systems.

8.2. Computer Input Devices

8.2.1. Classification of Input Devices

Input devices are used to read and enter input data and calculation programs into the machine memory. They are related to peripheral devices and are devices that support the man-machine communication process.

Input devices are usually divided into two groups--manual and automatic (Figure 8.2). Manual devices include those designed for manual (by means of a keyboard) entry of input information into a computer and automatic devices include those that receive information from a machine carrier (punch cards, papertapes and magnetic tapes), automatic reading machines, speech recognition devices and graphic information input devices.

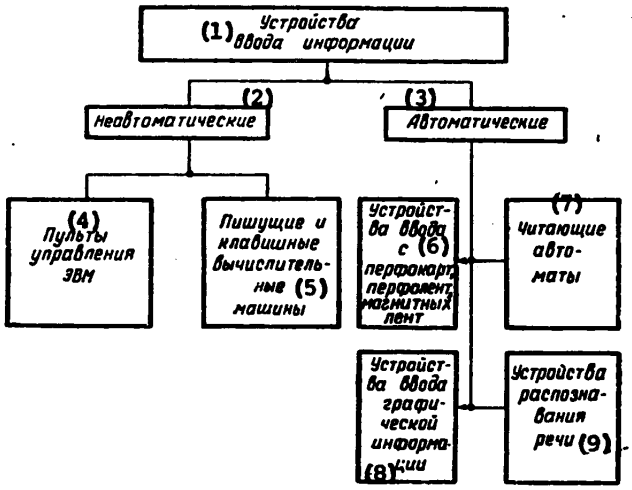

Figure 8.2. Classification Diagram of Input Devices

[Key on following page]

[Key continued from preceding page]:

1. Information input devices
2. Manual
3. Automatic
4. Computer control consoles
5. Typewriters and keyboard computers
6. Punch card, papertape and magnetic tape input devices
7. Automatic reading machines
8. Graphic information input devices
9. Speech recognition devices

The speed of information entry by using manual devices is low and is determined mainly by the operator's capabilities (not more than 20 characters per second). However, these devices are used extensively in modern computers operating in a time-sharing system when users are connected to the machine or system by communications lines using keyboard input devices.

Automatic devices enter information without human participation. They have higher input speeds and are used mainly to enter large information files.

Methods of reading information from machine carriers. Among automatic input devices, machine carrier information input devices--punch card and papertape--have become most widely used. Devices for reading from these carriers are designed to convert data recorded in the form of perforations to a system of electric pulses fed to the registers of the internal storage. Information is read from punched carriers by two methods--contact and contactless.

The contact, or electromechanical method consists in the following. The punched carrier is moved between the contact roller and metal brushes. The paper or cardboard insulates the brushes from the roller where there are no perforations and the electric circuit between the poles of the circuit is not shorted out. If there is a perforation, an electric circuit is formed by contact of the brush with the roller with the perforation and the current pulse is a signal to receive the numbers encoded in the machine carrier.

The contact method is also used when reading graphic marks entered on punch cards, dual-cards and special forms. When reading information from the indicated carriers, the contact brushes close the electric circuit in the presence of a graphic marker, as a result of which a signal is formed at the output of the readout unit. The contact method is used mainly in punch card input devices. Despite its reliability, it has the main disadvantage of limited reading speed that does not exceed 700 punch cards per minute.

The contactless method is used in most modern punched carrier readout devices. The contactless method considerably exceeds the reading speed compared to the contact method. Thus, for example, reading speed from punch cards reaches 1,000 cards per minute and from papertapes it reaches 1,500 lines per second in contactless input devices. This method is based on the use of photoelectric, capacitive or pneumatic methods.

The essence of the photoelectric method consists in the fact that the information carrier (punch card or papertape) moves between a light source and the reading head with several photosensitive elements. If there are perforations, a narrow beam of light focused by a cylindrical lens passing through the hole in the punched carrier impinges through a light guide onto the photosensitive element, which converts the light signal to an electric impulse. The number of photosensitive elements and light guides is determined by the number of tracks on the papertape or columns on the punch card.

The essence of the capacitive reading method consists in the fact that the punched carrier passes between capacitor plates in the reading device which are arranged opposite each track of the papertape or column of the punch card. The presence of a hole is signalled by variation of capacitance at the moment the hole of the punched carrier passes between its plates.

The pneumatic method is based on passage of an air jet through the holes of the punched carrier and its effect on the receiving element, which, being triggered, shapes a signal in an electric circuit.

8.2.2. Punch Card Information Input Devices

The most widely used punch card information input devices are YeS-6012, YeS-6013, YeS-6016, YeS-6019 and other devices used in the YeS computers. Let us consider reading and entry of data into the machine on the example of some of the enumerated devices.

The YeS-6012 punch card input device (USSR) is designed to enter information from 45- or 80-column punch cards. Information is read by this device by the photoelectric method. The punch card is fed by the narrow side. The input speed is 500 punch cards per minute. The capacity of the feed and receiving hoppers is up to 1,000 punch cards. Information is read column by column, synchronously with movement of the punch card in two modes:

reading of information encoded in KPK-12 code with equipment conversion of it to DKOI code;

reading of information encoded in any other code without equipment conversion.

The reading mode is selected by the input instruction code being fed to the device. For example, upon the instruction READ WITH CODE CONVERSION, information is read from the punch card with conversion of each column from 12-position KPK-12 punch card code to DKOI binary code.

Upon the instruction READ WITHOUT CODE CONVERSION, information is read from the punch card without conversion from KPK-12 to DKOI code and is transmitted in the form of two bytes: the first byte contains information of position 12-3 of the column (digits 2-7) and the second contains information of position 4-9 of the same column (digits 2-7). The zero and one digits of both bytes are filled with zeros.

Information is read by means of 12 photodiodes according to the number of punch card positions. Monitoring for a combination of perforations impermissible in KPK-12 code is provided during reading. This monitoring is accomplished when reading in the mode with apparatus code conversion simultaneously with formation of eight-digit combinations of DKOI code when signals from the photodiodes are fed to the code converter. The indicated monitoring is not carried out when reading information in the mode without conversion.

Monitoring of engagement of a punch card, nondelivery of a punch card to the read-out device, dual delivery of the same punch card and monitoring the synchronization circuits for completion of an information reading cycle from a punch card are carried out in any mode. If an error by a corresponding monitoring circuit is detected, a signal is emitted to the operator console. The console has the keys "START," "STOP," "END OF CARD FILE" and "RUN" and indicator lamps which light up when the monitoring circuit emits an error signal.

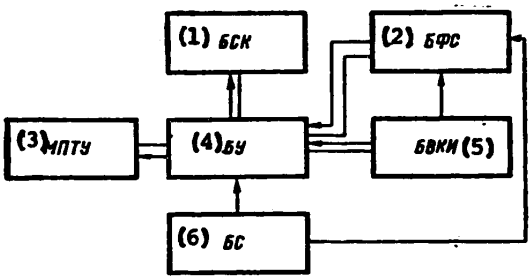

Figure 8.3. Block Diagram of Punch Card Input Device

Key:
1. Channel integration unit
2. Signal shaping unit
3. Punch card feed, transport and stacking mechanism
4. Control unit
5. Information receiving and verification unit
6. Synchronization unit

A block diagram of the punch card input device is shown in Figure 8.3. The diagram includes the following units: control unit (BU), punch card feed, transport and stacking mechanism (MPTU), information receiving and verification unit (BVKI), channel integration unit (BSK), synchronization unit (BS) and signal shaping unit (BFS). The units have the following designation:

the punch card feed, transport and stacking mechanism (MPTU) moves the punch cards through the photoelectric reading unit from the feed to the receiving hopper;

the information receiving and verification unit (BVKI) is designed to receive electric signals coming from each column of the punch card when information is being read;

the signal shaping unit (BFS) shapes the signals coming from the BVKI from each position of the punch card. The synchronizing unit (BS) shapes the synchronizing signals when reading information from each column and also synchronizes the operation of all circuits and mechanisms;

the control unit (BU) follows the passage of the punch cards through the card track, starts and stops the devices and coordinates the operation of the BSK, BS and BVKI;

the channel integration unit (BSK) connects the device to the input-output interface and through it to the selector or multiplex channel.

The YeS-6013 punch card input device (USSR) is designed to read information from 80-column punch cards. It is made the same as the YeS-6012 device and has identical principle and information reading modes. The distinguishing feature of this device is an increase of the input speed to 1,200 punch cards per minute and capacity of the feed and receiving hoppers up to 2,500 punch cards.

The YeS-6016 punch card input device (CSSR) is used to read information from 80- or 90-column punch cards. The readout modes are the same as in the YeS-6012 and YeS-6013. Unlike the YeS-6012 and YeS-6013, the YeS-6016 device is a buffered device having a memory buffer containing information from two punch cards. The maximum input speed is 1,000 punch cards per minute. The capacity of the feed hopper is 2,000 punch cards and that of the receiving hopper is 2,500 punch cards. Information is read by the photoelectric method column by column and the result of reading is placed in a buffer storage device. The YeS-6016 device has supplementary instructions which are used to fill the buffer storage device with binary information from the internal storage.

The YeS-6019 punch card input device (USSR) is distinguished from the other devices by the punch card feed method. Instead of mechanical feeding of punch cards (using blades), it has vacuum feed. The input speed is 1,200 punch cards per minute. The device has a single feed hopper with capacity of 2,000 punch cards and two receiving hoppers with capacity of 2,000 and 300 cards.

8.2.3. Papertape Information Input Devices

These devices are used to enter numeric and alphanumeric information encoded on a machine carrier--papertape--into the computer.

The domestic papertape input devices include the FSU-1, FSM-3, FSM-5, U-225, UV1-23, YeS-6022 and so on. The contactless method, using photoelectric or capacitive sensors, is employed to read information from papertape in most modern computers. The devices in which the indicated method is used read the information sequentially by lines, in each of which one of the symbols is encoded. The information entered on the papertape is read in files during a single input operation. Let us consider one of the devices used in the YeS computers.

The YeS-6022 papertape input device (USSR) is designed to enter information from a five-, six-, seven- and eight-track papertape and can be used as any of the models of the YeS computers. Information is entered on the tape in KOI-7 code (GOST 13052-74) and is read photoelectrically at a speed of 1,500 lines per second.

The operation of the device is controlled from the operator's console. The operator can control the following operating modes of the device:

input mode--multiplex or monopole;

input information verification mode for evenness, oddness or reading information without verification;

input mode of five-, six-, seven- or eight-track tapes;

information input blocking mode from any track of the papertape and so on.

Information can be entered by two types of input instructions: with conversion of KOI-7 code to DKOI code or without code conversion (copy mode) that permits information to be entered in the machine in any code.

Different types of verification are provided in the input device: for engagement of the papertape, regulation of the papertape transport mechanism, loss of symbol when the papertape is stopped, entered information for evenness and oddness, errors in symbol code and malfunctions in equipment.

The YeS-6022 device permits information to be entered from short segments of the tape 0.1-10 meters long without attachments. Papertapes up to 300 meters long are entered by means of a feed cartridge.

8.2.4. Information Input Devices From Machine-Readable Documents--Automatic Reading Machines

An automatic reading machine is a device capable of reading and entry of information into a machine directly from primary documents, changing the intermediate carriers (punch cards, papertapes and magnetic tapes). The information carriers for automatic reading machines are machine-readable documents--standardized forms, which combine primary documents and machine carriers. Let us briefly consider methods of encoding the information on these carriers.

The standardized form is a sheet of paper of specific dimensions on which a matrix separating the sheet into vertical rows and horizontal lines is imprinted typographically. As was mentioned earlier, the recording is made by means of graphic markers at special types (coded, stylized and normalized). The information can be imprinted with a simple pencil and also with ordinary or magnetic inks.

The graphic marks are entered in specific locations on the form in pencil. The digit capacity of the information determines the location of arranging the graphic mark in the line of the form. Information can be represented in different codes: binary, binary-decimal, decimal and so on. Selection of the encoding system depends on different factors and primarily on the laboriousness of encoding. Information is encoded in graphic markers in Soviet practice on A4 forms (210 X 97 mm).

A specimen of recording the number 1,282 by graphic marks on a standardized form in binary, binary-decimal and decimal codes is shown in Figure 8.4.

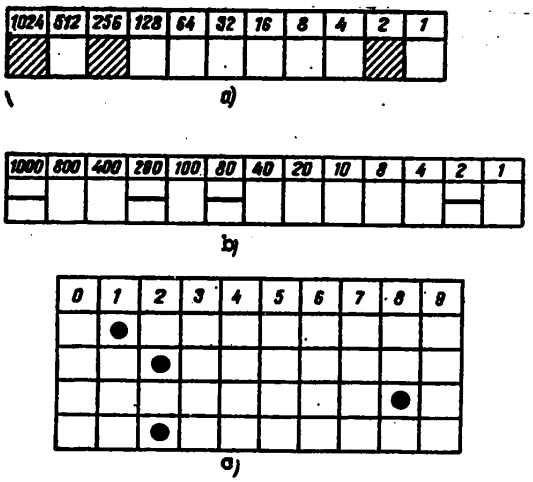

Figure 8.4. Encoding of Number 1,282 by Graphic Marks in Different Codes: a--in binary; b--in binary-decimal; c--in decimal

Code type is a type in which the characters are shown by the number of points of different diameter or hatches of different length and thickness. The code marks can be entered on the form by ordinary typographic ink or magnetic ink together with depiction of the sign with ordinary type. There are several code types, for example:

Broidot type in which characters are encoded with five vertical lines of different length located under numbers;

Steinometic type in which the character code is printed in the form of a combination of points 2.2 mm in diameter arranged on four horizontal lines. With this method of encoding the readout device recognizes the code marks rather than the written character itself.

Stylized type is a type in which the characters distinguished from ordinary types are easily detected by identification devices and also when reading them visually.

Stylized types are divided into those for optical and magnetic methods of reading. SMS-7 alphanumeric magnetic type (GOST 16394-70) is mainly used in our country. This type contains 10 numbers (0-9), letters of the Russian and Latin alphabets and five service symbols. Each character is formed by seven vertical lines of identical width, but of different length. The lines are separated from each other by six different intervals (wide and narrow). The combination of the lines and intervals forms the microcode of the character. The combinations of intervals form the number and letter code. When characters are encoded, the narrow interval is taken as a zero and the wide interval is taken as one and thus any character is represented by a binary code. The advantage of SMS-7 type compared to other stylized magnetic types is the use of the digital method of reading, which has

simplicity and reliability. An example of numbers recorded by SMS-7 stylized magnetic type is shown in Figure 8.5.

Figure 8.5. Example of Recording Numbers with SMS-7 Stylized Magnetic Type

As was mentioned earlier, normalized type is written by hand in special normalizing rectangles in black ink or India ink. There are several normalized types. A normalized type developed by the NII TsSU SSSR [Scientific Research Institute, Central Statistical Administration of the USSR] is shown in Figure 8.6. There are diagonal, median and vertical lines in each rectangle of this type. The rectangles and lines are written in red undetectable by the photoelements. Each number is read by means of 10 photodiodes.

The presently existing automatic reading machines are capable of identifying a limited set of written characters. Their operating principle consists of performing the following basic operations: inspecting the image of the written character, compilation of its description and comparison of the description to a standard. In general form the structure of the automatic reading machine consists of the sensing unit, memory unit, comparison device and resolving device. The sensing unit displays the image in the form of electric signals, as a result of which a code is formed, i.e., the image is described. The comparison device compares the description of the image to standards stored in the memory unit. The resolving device identifies the description with one of the standards according to the adopted rule and emits a coincidence or refusal signal at the output. The structure of the automatic reading machine depends on the adopted methods of character recognition. There are different methods of recognition. The most widespread are the following: comparison to a standard, following the contour of the character and separating the fragments of the character.

Depending on the type of types written on the standardized form, all automatic reading machines can be divided into two groups: automatic machines designed to read magnetic types and automatic optical reading machines.

Automatic reading machines designed to read (identify) magnetic types include those for reading written characters entered on forms in magnetic dyes or inks. Domestic devices of this type include the complex of devices for printing, reading and sorting documents. The information subject to entry in this device is entered with SMS-7 type. The operating principle of the device consists of the following. The characters are magnetized prior to readout. As the form moves under the magnetic reading head, the magnetic field of the character creates a signal of specific amplitude and shape at the output of the reading device which is compared to the reference signals stored in the memory of the automatic machine. The read character is identified as a result of comparison. The read information is retrieved to the

computer by the unit for conversion of SMS-7 code to computer code. The document sorting device has 12 receiving hoppers and permits selection of forms with features equal to the given number or lesser and greater than the given number. Its productivity is 720 forms per minute.

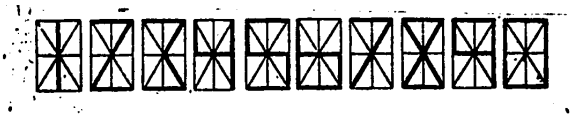

Figure 8.6. Normalized Type Developed By Scientific Research Institute, USSR Central Statistical Administration

Automatic optical reading machines are designed to read graphic marks and coded, normalized and stylized types.

Soviet automatic optical reading machines designed to read graphic marks include the Blank device (Blank-1, Blank-2 and Blank-P). This device was used widely in developing the materials of the All-Union census of 1970 and 1979.

A device of the Blank type consists of a document feed and transport mechanism, photoelectric reading unit, verification unit and read form receiving mechanism.

The operating principle of the device consists in the following. Forms are fed to the readout unit from the feed hopper with capacity of 700 forms by means of the form transport mechanism, where the information is read, and is then fed to the verification unit to verify the read information for evenness of marks in the line. With correct reading of the hatcher marks, the forms are fed to the receiving hopper and if reading is incorrect they are fed to the rejection hopper. The device can operate both jointly with a computer and in the self-contained mode to rerecord information from forms to magnetic tape.

Information is read by means of photoconverters from 26 columns of the form simultaneously. The reading speed is 9,000 forms per hour.

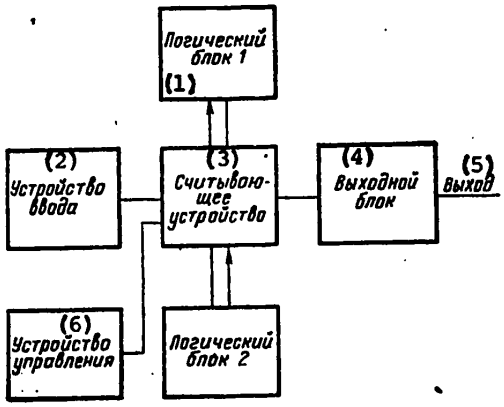

Figure 8.7. Block Diagram of Ruta-701 Reading Device

[Key on following page]

[Key continued from preceding page]:

1. Logic unit
2. Input device
3. Reading device
4. Output unit
5. Output
6. Control device

Soviet devices for reading normalized types include the Ruta-701 device. This device is designed to read digital information and four service symbols, which are entered on forms manually in black India ink or typographical ink with a typewriter. The operating principle of the device consists in the fact that the form fed to the input device (UVv) by the feed mechanism is fed to a transporter and is moved under the reading chamber in which the characters are examined and a description of their image is compiled. The reading device (SU) can operate in two modes: in the retrieval scanning mode in which information is retrieved and controlled by the feed mechanism, and in the operating scanning mode when the characters are examined and received and a description of the image is entered in the logic unit (LB) of the device. The characters are converted from visual form to a system of electric signals by means of "travelling wave" scanning. When characters are being read, a section of the form is examined by scanning by projecting a light beam onto the form. The reflected light impinges on photomultipliers from whose output electric signals are fed to a video unit. These signals correspond to shaded sections illuminated by a light beam. The different output signals will also correspond to the sections of the form with different degree of shading. The output electric signals are identified comparing them to standards located in the storage device of the automatic reading machine.

A block diagram of the Ruta-701 reading device is shown in Figure 8.7.

8.3. Computer Output Devices

8.3.1. Classification of Output Devices

Information output devices are designed to retrieve from the computer the results of calculations and intermediate data in the form of encoded perforations on machine carriers and also for printing and on screens.

These devices can be divided into two main groups:

information output devices on machine carriers (punch cards, papertapes and magnetic tapes);

output devices of information in the form of text, graphs and images, i.e., devices that permit information to be printed and retrieved to screens.

The classification of information output devices is shown in Figure 8.8.

8.3.2. Punch Card Output Devices

The most widely used punch card information output devices for recording and storage of intermediate or final results are YeS-7010, YeS-7012 and YeS-7013 devices used in third-generation computers. These devices can be connected by means of

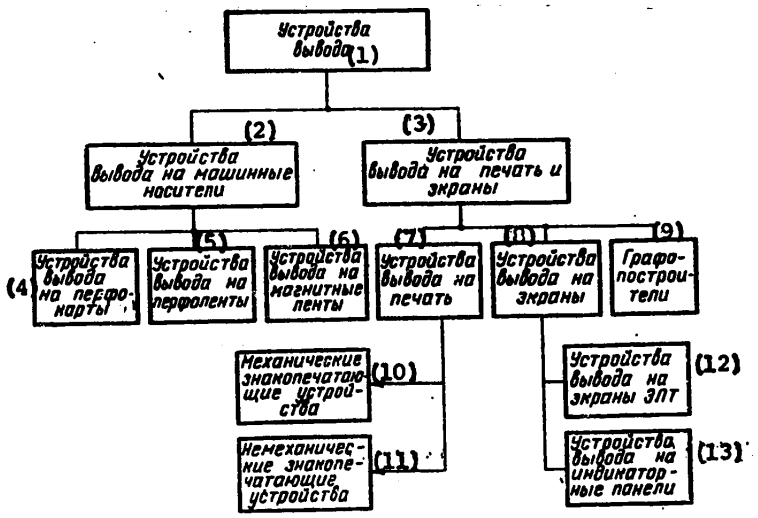

Figure 8.8. Classification of Information Output Devices

Key:

1. Output devices
2. Machine carrier output devices
3. Printed and screen output devices
4. Punch card output devices
5. Papertape output devices
6. Magnetic tape output devices
7. Printed output devices
8. Screen display devices
9. Graph plotter
10. Mechanical printing devices
11. Nonmechanical printing devices
12. Output devices to cathode-ray tube screens
13. Output devices to display panel

an input-output interface to the multiplex or selector channel of any model of the YeS computers.

Position perforation with step movement of the card with the wide side under the perforating mechanism is accomplished in the indicated types. This method is more productive than the column perforation method.

The YeS-7010 punch card output device (USSR) is a card position perforator designed to retrieve information from a computer to 80-column punch cards.

The YeS-7010 device has a buffer storage (BZU) with capacity of 256 bytes with maximum amount of information in 160 bytes. The perforation speed is 100 punch cards per minute. The capacity of the feed hopper and of two receiving hoppers is 700 punch cards, respectively. The perforations are made line by line, i.e., for each position.

The card perforator can operate in the information output mode in KPK-12 code with preliminary conversion from BKOI code and in any code without conversion.

Of the two stackers, one is used to receive correctly perforated punch cards and the other is used for reject punch cards. The card perforator provides perforation for all positions of the card with entry of up to 672 perforations on it, i.e., with filling coefficient up to 0.7.

Monitoring the filling of punch cards, non-feed from the stacker or double feed and checking the evenness of information in the buffer storage are provided in the punch card. If an error is detected during perforation, the card is stacked in the first stacker. Sending the punch cards to the first and second stackers with recording with code conversion and without code conversion is provided by instructions of the YeS-7010 device. The punch cards are sent to one or another hopper by means of a sorting device. The punch cards move intermittently under the perforator with a stop at each position for perforation.

The perforator has a 14-position operating cycle. One punch card is fed to the machine during each cycle with an interval of one position behind the previous one.

Let us consider the operating principle of the perforator by the functional diagram shown in Figure 8.9. Each punch card covers the route in five cycles from the moment it is grabbed by the feed knife to stacking in the stacker.

During the first cycle the first (bottom) punch card is grabbed by the feed knife and is fed to the first pair of transport rollers I by means of which it is fed to the second pair of rollers II. During the second cycle the punch card is fed by the second pair of rollers to the perforator, consisting of 80 male and female dies.

During the first cycle the punch card passes between the female and male dies and is fed by a third pair of rollers III to the brush unit. The perforation process is completed during this cycle. Current pulses are fed to the perforation electromagnets 1 with reading of information from the buffer storage. If the perforation electromagnet is switched on, the armature 2 is tightened,which rotates a pawl 7 through a lever 3, feeding it with the groove under the impact plate 4. The plate makes a forward-reverse motion upwards and downwards by means of an eccentric shaft 10. When it is lowered down, it impacts with the striker 5 on the pawl and pushes it downward together with the male die 8. The male die, passing into the hole of female die 9, punches a hole in the card located under themale and female die. Being raised, the plate returns the pawl 7 together with the male die to the initial position by means of stop 6 and the punch card is moved to the next position. Perforation is again made in the other position in the sequence described above.

During the fourth cycle the punch card passes through the brush unit and is fed by the fourth pair of rollers IV to the sorter. During this cycle the perforations are perceived by contact of the brushes with the contact roller through the perforations, i.e., the perforations are read for checking their presence.

The fifth cycle is stacking. Depending on the response of the sorting electromagnet, the punch card is fed to the first stacker or is sent by the fifth pair of rollers V to the second stacker.

The YeS-7012 punch card output device (USSR) can be connected to any model of the YeS computers. The method of perforation in the device is the same as in the

YeS-7010. The rate of retrieving information is 250 punch cards per minute. The capacity of the feed magazine and of the two stackers is 1,200 punch cards each. The buffer storage has a capacity of 256 bytes.

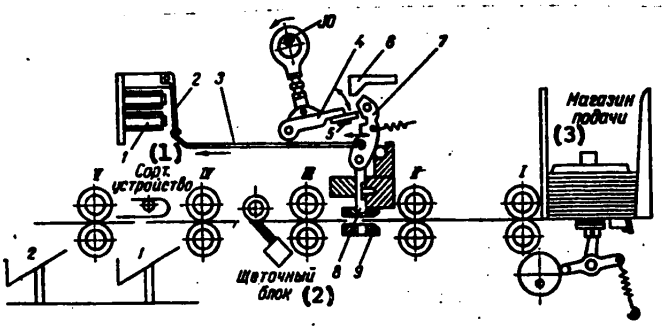

Figure 8.9. Functional Operating Diagram of YeS-7010 Device

Key:
1. Sorter
2. Brush unit
3. Feed magazine

The distinguishing feature of the YeS-7012 device is verification of perforation during a current recording operation and also the presence of verification of an impermissible combination of perforations when the perforation is made in the code conversion mode. A combination which contains more than one perforation in positions 1-7 of any column of the punch card is regarded as impermissible.

The YeS-7013 punch card output device (CSSR). The designation, method and modes of perforation are similar to the YeS-7010 and YeS-7012 devices. The difference is that the capacity of the buffer storage is increased (by two punch cards) and the capacity of the hoppers is increased--up to 1,500 punch cards for the feed magazine and up to 1,300 punch cards for the two stackers. Perforation is verified by the photoelectric method of reading the perforated cards.

8.3.3. Papertape Output Devices

These devices are designed to retrieve information from a computer to paper punch tapes. Devices of types YeS-7022 and YeS-7024 are used in models of the YeS computers. These devices are designed to retrieve information to a five- or eight-track papertape.

The information retrieval speed is 150 lines per second (YeS-7022) and 100 lines per second (YeS-7024).

Passage of the symbol is verified in the indicated devices by its information channels and the presence of pulses is also verified. Information retrieval to the papertape can be accompanied by supplementing the number of perforations of each symbol to evenness or oddness. The corresponding mode is controlled by means

of a switch installed on the console of the device. Information is retrieved to an eight-track papertape in the mode of conversion from KOI-8 to KOI-7 code (GOST 13052-74) and is retrieved to a five- to eight-track papertape in the copy mode.

The output devices inform the computer system of its status by transmitting status bytes to it. The devices perform the following instructions: RECORDING, DATA AND SYMBOL RECORDING, END OF BLOCK and NO-LOAD.

Besides the enumerated devices, the YeS-7902 papertape input-output station, which consists of a control device and papertape information input-output devices connected to it, is available in the YeS computers for retrieval to papertape. Three devices can be connected--two papertape input devices and one papertape output vice. The YeS-7902 papertape station can be used in any model of the YeS computers.

8.3.4. Information Printing

Information printing is the most widely used method of information retrieval. Compared to the other methods, it has the advantage that finished documents with input data and the results of calculations printed on them are retrieved from the machine.

Printers can be divided into two groups by operating principle--sequential printing and parallel printing devices.

The information is printed in sequential printing devices by sequential recording of characters. Electric typewriters, bookkeeping and billing machines and telegraph equipment have become most widely used among this group of devices.

Parallel printing devices are more widespread. The entire line is printed during one operating cycle in these devices, which provides high recording productivity. Therefore, they are called high-speed printers.

The main characteristics are the number of different characters used and also the number of characters per line and printing speed.

The most widespread actuating elements of parallel printing devices are type bars and type wheels. Recording of information using bars is used in low-speed printers, whose speed is 100-150 lines per minute.

The most widely used method of recording information in computers is recording by means of a type wheel using the dynamic principle of printing in which characters are printed continuously at constant speed.

The principle of recording consists in the following. Printing wheels of the same type, assembled on the same axle in the form of a cylinder, rotate at constant speed. There may be from 128 to 160 print wheels along the length of the cylinder, each of which represents a specific digit of the printer. A specific set of characters (Figure 8.10), by means of which the symbols are imprinted on paper, is engraved on the wheels. The set of characters for each of the printers is constant. The characters are printed during rotation of the cylinder when the type character 1 passes the hammers 2 of the striker mechanisms. A red ribbon 3 is located between the hammers and characters and paper 4 is located above it. The hammer 2,

striking the paper through the red ribbon, presses it against the type character, as a result of which the symbol is imprinted on the paper.

The entire line is printed within several cycles. A specific number of symbols is printed during each cycle along the length of the line at different intervals. Thus, all the necessary information of the line is recorded after completion of the last cycle. This information is preliminarily stored in the UVU storage device in the form of a code used in the given device. At the same time a code disk resting on it on one shaft rotates as the cylinder rotates. During rotation this disk emits signals to the UVU which are the character code passing at a given moment of time above the striker hammers. Each symbol has its own code. The printed symbol code stored in the memory and the symbol code retrieved by the code disk are analyzed in the comparison register. If there is agreement, the electromagnet 5 responds, which tightens armature 6, setting the hammer in motion, and printing is accomplished. Each printing digit is assigned its own address for storage of the code in the storage device and thus the information is printed in the required digits.

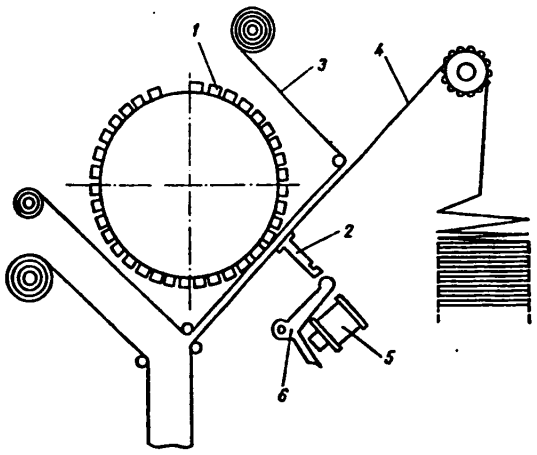

Figure 8.10. Printer Digit

After one line is printed, the paper is transported by one or several spaces depending on the given mode. The paper transport mechanism is controlled by program by means of a control papertape. The combination of code perforations on this papertape denotes the paper transport mode. After return of the paper, the device is ready for printing the next line.

All ATsPU [alphanumeric printers] of the YeS computers are cylinder (wheel) type devices. The information for printing is fed to a buffer storage from the channel. Information is verified for evenness simultaneously with storage of it in the buffer storage.

Devices with dynamic printing principle include alphanumeric printers (ATsPU) used in the following models of YeS computers: YeS-7030, YeS-7031, YeS-7032, YeS-7033,

YeS-7034, YeS-7035 and YeS-7038. The enumerated ATsPU are cylinder type devices in which the symbol character is a set of cylinders resting on a common shaft with complete set of characters on each cylinder. The printing speed is 600-1,100 lines per minute.

Printing is accomplished on roll paper 80-420 mm wide at a speed of 650-900 lines per minute. Up to 128 symbols are printed in each line. Any of 83 basic symbols or a single service symbol can be printed on each position of the line. The symbols can be numbers, letters of the Russian and Latin alphabets and special characters.

The YeS-7030 and YeS-7032 ATsPU (USSR) consist of a control device and their own printer. The control device represents in turn combination of the integration unit with the channel and its own print control device. The YeS-7030 and YeS-7032 alphanumeric printers include the following mechanisms and units--channel integration unit (BSK), recording control unit (BUZ), print control unit (BUP), mechanism control unit (BUM), printing mechanism (PM) and buffer storage (BN).

Alphanumeric printers are buffer type devices having a memory to store data on one line. The buffer storage (BN) has a capacity of 128 bytes. When printing, the alphanumeric printer performs the following functions: reception and storage of data line by line, reading and printing of data and moving the paper by a given number of lines.

The information subject to printing is fed from the channel integration unit (BSK) to the recording control unit (BUZ) and then to the buffer storage (BN). The recording control unit (BUZ) controls and maintains the two main operating modes of the device--recording and printing. In the recording mode, data are received from the BSK through the BUZ and they are recorded in the BN. After data are recorded in the BN, the device is switched to the printing mode during which the information located in the BN is printed on one line of papertape. Upon rotation of the cylinder, signals are transmitted from the BUM to the BUT to form the code of the cylinder line which passes under the print hammers.

The specifications of alphanumeric printers of the YeS computers are presented in Table 8.1.

8.3.5. Graph Plotters

Due to its descriptive nature, graphical information is convenient for perception by man and therefore has wide application in different areas of science and technology. Automation of the processing of this information using computers is of important significance. One of the means of automating the processing of graphical documentation is the use of graph plotters.

Graph plotters are papertape graphic and text information output devices. They are used to make drawings of electric circuits and also of the results of calculations in the form of graphs and curves.

Graph plotters are roll or plotting board type graphic recording devices.

Table 8.1. Specifications of Alphanumeric Printers of YeS Computers

ATsPU Specifications	YeS-7030 (USSR)	YeS-7031 (GDR)	YeS-7032 (USSR)	YeS-7033 (PNR)	YeS-7034 (CSSR)	YeS-7035 (GDR)	YeS-7038 (CSSR)
Printing speed, lines/min	650-900	900	900	600-1,100	900	600	750-1,000
Number of symbols per line	128	156	128	120, 126 160	132	120	160
Number of characters on cylinder	84	64	84	64	64	64	64
Buffer storage	Available						
Operating Mode	Multiplex and selector						
Time interval of moving paper for next line, ms	10	6	10	4-5	8	6	8

A wide papertape is used as the information carrier in roll type devices and sheets of paper measuring 1,000 X 1,500 mm are used in plotting board devices.

Graph plotters can be connected directly to a computer or can operate in the autonomous mode. Information is exchanged between the computer and graph plotter integrated with the computer through channels through a standard input-output interface. When working in the autonomous mode, data are fed to the graph plotter from papertape or magnetic tape.

Graph plotters operating as peripheral devices of YeS computers are used in economic information processing systems. They include the YeS-7051, YeS-7052, YeS-7053 and YeS-7054 graph plotters having an electric typewriter part and electronic system of graphic data reception and processing.

The electromechanical part is a two-coordinate recording plotter (DRP) that provides step by step movement of a typing mechanism over the paper carrier, which may consist of several typing elements of different colors.

The electronic system of data reception and processing receives the graphic program in the buffer storage (if it is present) or in the data processing unit, decodes orders and controls the actuating channels of the DRP.

A photoreading device (FSU) is connected to graph plotters of the YeS computers operating in the autonomous mode for entry from papertape and the YeS-7050 reading device is connected for entry from magnetic tape. When working with computers, graph plotters are connected to the selector or multiplex channels and operate under program control.

The operation of graph plotters is controlled according to instructions. For example the SYMBOL DRAWING instruction sets the mode in which graphic images of symbol codes are drawn on paper.

Some models of graph plotters are equipped with a character generator, which draws only a specific set of symbols corresponding to a given code. Other models having buffer memory describe the symbol graphically on a coordinate grid according to programs stored in the memory.

Let us consider the operating principle of graph plotters on the example of the YeS-7051 model.

The YeS-7051 graph plotter is an electromechanical plotting board device with working field 1,000 X 1,050 mm and speed of 50 mm/s. It consists of a two-coordinate recording plotter (DRP), plotter control unit (BUP) and data conversion unit (BPD).

Graphical information can be entered only from a computer (in the channel connection mode) or from papertape and magnetic tape (in the autonomous mode). The DRP includes a crosspiece and carriage with writing mechanism that is shifted along the crosspiece. The crosspiece moves the writing mechanism in the direction of the X axis and the carriage moves it in the direction of the Y axis.

Table 8.2. Characteristics of Graph Plotters of YeS Computers

Device	Spacing of Writing Element, mm	Maximum Drawing Speed, mm/s	Type of Graph Plotter	Dimensions of Working Field, mm	Ribbon Colors	Set of Symbols
YeS-7051 (USSR)	0.05	50	Plotting board	1,000 X 1,000	3	253
YeS-7052 (USSR)	0.1; 0.05	200	Roll	380 X 600	3	64
YeS-7053 (USSR)	0.1	150	Roll	841 X 1,600	3	253
YeS-7054 (CSSR)	0.05	100	Plotting board	1,600 X 1,200	4	96

Graphical information is entered in the buffer memory with capacity of four Kbytes. The information is received by the BPD. It also performs line and circular interpolation, i.e., it controls the motion of the writing element in a straight line or along the arc of a circle and controls the step motors through the BUP. The BPD contains a line-circular interpolator (LKI), which determines the motion trajectory, and a line type block (BTL) to control the writing mechanism in the DOTTED LINE and DOT-DASHED LINE modes. The BPD draws up to 253 symbols in the code of the YeS computer, controlled by means of a program. The symbols are drawn at different angles of inclination (up to 16 angles).

The writing mechanism has three elements (automatic recorders) that provide a three-color image of lines of three types--continuous, dotted and dot-dashed.

The characteristics of the graph plotters are presented in Table 8.2.

8.4. Operator-Computer Communication Devices

Operator-computer communication devices, as was already mentioned, are designed for two-way exchange of information between man and computer. Alphanumeric and control information is usually entered in these devices by a set of keyboard typewriters. Printers, cathode-ray tube (ELT) screens and display panels are used for information input-output.

The keyboard together with the printer represents a typewriter installed on the operator consoles (a console typewriter) and a keyboard in combination with an ELT screen or display panel represents an electronic information display device.

Typewriters are the simplest devices for operator-computer communication but they have a low rate of information exchange. The advantage of information display devices is the descriptiveness of displaying information and the higher speed of retrieving it compared to a typewriter.

8.4.1. Console Typewriters

Operator consoles are equipped with electric typewriters. Their printers have different design principle--type levers, type wheels and electrothermal devices. The most widely used are printers with type levers.

The YeS-7070, YeS-7071, YeS-7073 and YeS-7074 devices, designed to operate as an operator console in models of the YeS computers, have become most widely used in modern computers. Using the typewriter keyboard, the operator can enter information into the computer and at the same time can print it on paper. Data are printed on paper when information is retrieved from the computer.

Besides the enumerated functions, console typewriters can perform initial loading of the program, interruption of the system and switching the power supply on and off.

Console typewriters consist of a sequential printing mechanism, keyboard that includes letter, number and special symbol keys, control and display members, control devices that connect the typewriter to channels and that control the operation

of the device itself. Konsul-260 typewriters (in YeS-7070 and YeS-7071 devices), Maritsa-141 typewriters (in the YeS-7074 device) and Zoyemtron-34-529 typewriters (in the YeS-7073 device) are used as the printing mechanism.

Console typewriters differ slightly in their specifications from each other in the makeup of characters on the keyboard and control and display members. However, there is an identical basic state of the devices in all the typewriters--set of instructions, algorithms for fulfilling them and organization of operation verification.

The printing speed of all the typewriters is up to 10 characters per second, while the number of characters per line is different--106 in YeS-7070 and YeS-7071 devices, 117 in the YeS-7072 device and 123 in the YeS-7074 device. The printing mechanisms have 46 type levers that permit printing of 1 of 92 characters in each position of the line.

The number of copies is 5-8, the width of the paper roll is 280-320 mm, the distance between characters in the line is 2.6 mm and the distance between lines is 4.5 mm.

One of the main units of console typewriters is the channel integration unit (BSK), which connects the device to the input-output interface and exchanges information with the channel. This unit verifies the incoming information for legibility, converts DKOI code to KOI-7 code and carries out reverse conversion.

When information is entered, the operator enters each symbol represented in KOI-7 code in the device by pressing the keys. The encoder converts this code to DKOI code and transmits it to the data register and then to the channel. When information is retrieved, the code taken from the channel passes through the decoder and is fed to the corresponding electromagnet of the electric typewriter, as a result of which the corresponding character is printed on paper.

All console typewriters have a systematic set of keyboard characters used in operating systems of the YeS computers and in basic programming languages, which provides the capability of using any console typewriter in any model of the YeS computers.

8.4.2. Electronic Information Display Devices

Information display devices include cathode-ray tube (ELT) information output devices. These dialogue ELT information display devices are frequently called displays or screen consoles. They are a convenient means of man communicating with the machine and have wide application from simple reference data service devices to the most complex information control systems.

The main advantage of dialogue display devices is the capability of working in the real-time mode.

The use of a buffer storage and special units permits these devices to be used as information input-output devices in data processing systems operating in the time-sharing mode.

If these devices are available, the operator can enter the required information into the computer by means of a keyboard or "light pen" (pencil) and can retrieve any information stored in the computer memory. In this case entry of information can be verified visually since the information is lighted up on a screen. Information is retrieved from the machine on the same screen and corrections can be entered in the information by means of the keyboard or "light pen" (pencil), after which the corrected information is again entered in the machine.

When using screen consoles, it is no longer necessary to prepare machine carriers (punch cards and papertapes) for entry of inquiries into the machine and accordingly the time required to receive answers is reduced.

In the collective-use mode, the capability of a large number of users to have access to the computer is available by using displays with modern computers.

Depending on the type of information displayed on the ELT screen, displays are divided into text (alphanumeric) and graphic. They can be divided into two groups by the method of control:

devices having direct output to the computer channel and operating under the control of channel instructions;

devices that use minicomputers as the control unit.

Text displays are alphanumeric information input-output devices. They are designed to display symbolic information and different symbols. Displays that display 500-4,000 characters on the screen have now been developed. Text displays can be used as single consoles connected to the computer channel and also as group complexes with a large number of screen consoles and group control unit. Both one and the other type of displays can be used as terminal devices in remote data processing systems.

The basic devices of a text display are display device (ELT), buffer storage (BZU) and keyboard which is used to enter text onto the screen. The display can also include a typewriter for printing the information to be processed.

The information entered on the screen is recorded in the BZU and is transmitted after visual verification by the operator through the communications channel to the computer. Information can also be entered on the screen by using a "light pen" (pencil).

Data are transmitted from the buffer memory of the display to the computer when operating in the reading mode and from the computer to the buffer memory of the display when operating in the record mode.

Text displays can operate both in the autonomous mode and in the computer communication mode. The maximum speed of information exchange is 100 Kbytes per second. The capacity of the text display screen is different for different models of computers and comprises 240-1,024 characters. Each line contains 40, 64 or 80 characters.

The basic models of text displays used in YeS computers include the YeS-7061, the YeS-7063 and the YeS-7906 complex. The characteristics of text displays are presented in Table 8.3.

Let us consider the operating principle of text displays based on the YeS-7906 model.

The YeS-7906 complex is designed to enter, retrieve and process (edit) alphanumeric information when operating in the YeS computers. The YeS-7906 complex includes the YeS-7566 group control device, up to 16 YeS-7066 portable consoles and a Konsul-260.1 typewriter. The portable consoles can be separated at a distance up to 600 meters from the control device. Portable screen consoles are designed to display alphanumeric information on the screen of a cathode-ray tube and to compose and edit it by means of a keyboard. A typewriter is connected to the YeS-7566 device by a special lead.

Portable consoles are connected to the channels of YeS computers by standard interface lines. A portable console consists of two basic parts--a cathode-ray tube display and keyboard.

The display has screen dimensions of 320 X 180 mm and a green glow color. The displays can be distributed in a maximum of four directions. When from 2 to 10 portable consoles are connected in series in one direction, the last console is installed at a distance of not more than 300 meters from the control device. If one portable console is connected to the direction, the maximum distance at which it is installed is 600 meters. The total capacity of the screens is 3,840 characters. The permissible capacity of the screen of each display is 960, 480 or 240 characters arranged in the following formats: 12 lines of 80 characters each, 6 lines of 80 characters each or 12 lines of 40 characters and 6 lines of 40 characters each, respectively. The set of permissible symbols is 96 characters.

The keyboard is equipped with two registers, 22 control keys and 40 alphanumeric keys.

The Konsul-260.1 typewriter is used only as a printing mechanism to produce printed copies. It has its own address and buffer storage and can be used both for autonomous data printing from all displays of the complex and for independent operation under channel control. Moreover, individual connection of typewriters to displays is permitted to achieve autonomous printing.

The YeS-7566 group control device has two buffer memory units designed to store the information of portable consoles and the typewriter.

The buffer memory unit of the portable consoles has its own internal storage on magnetic cores with capacity of 4,096 bytes.

The buffer memory unit of the typewriter has a capacity of 1,024 bytes.

Graphic displays provide input-output of graphic and alphanumeric information on an ELT. They are used widely in machine editing systems, in scientific research

Table 8.3. Characteristics of Text Displays of YeS Computers

Device	Maximum Number of Displays	Screen Capacity, Characters	Screen Format, Lines/characters	Number of Symbols in Set	Buffer Storage, bytes	Capability of Producing Printed Copy
YeS-7061 (Hungary)	1	1,024 960	16 x 64 12 x 80	64	1,024	No
YeS-7063 (Hungary)	1	1,024 960	16 x 64 12 x 80	96	1,024	Yes
YeS-7063 (CSSR)	1	960	12 x 80 24 x 40 15 x 64	96	1,024	Yes
YeS-7906 Complex (USSR)	16	960 480 240	12 x 80 6 x 80 12 x 40 6 x 40	96	4,096	Yes

and when modelling dynamic processes. Like alphanumeric displays, they can be used as single consoles and group complexes.

The graphic display includes and ELT display with high-speed deflection systems, buffer memory, character generator, vector generator, alphanumeric keyboard, functional keyboard and "light pen" (pencil).

The operating modes of the graphic display are controlled by an instruction system. The main operating modes are as follows:

absolute mode--to light up points or vectors on any absolute coordinates of the screen;

character mode--to form and retrieve characters on the screen;

graph mode--to reproduce curves with fixed spacing along the X axis and with arbitrary spacing along the Y axis;

arc mode--to reproduce arcs of circles.

The image on the graphic display screen is first described by a display instruction system and is placed in its buffer memory.

Let us consider as an example the main characteristics of the YeS-7064 graphic display used in models of the YeS computers.

The YeS-7064 graphic display is a graphic and alphanumeric information input-output device based on a cathode-ray tube. This device is used jointly with models of high-capacity YeS computers in solving problems in which the input data and intermediate or final results are conveniently represented in the form of drawings and graphs. Data is transmitted at a speed of 1,200-4,800 bits per second.

The YeS-7064 device consists of an electronic console consisting of a display with cathode-ray tube, alphanumeric and functional keyboards, "light pen" (pencil), buffer memory with capacity of 8 Kbytes and control device.

The control device consists of display control units and an information processing unit. It is used to match the operation of all the units and controls the operation of the display in various modes.

The alphanumeric and functional keyboard and "light pen" (pencil) are input devices.

The image is formed by means of a character generator, vector generator, character memory unit and display. As in text displays, data are transmitted from the computer to the buffer memory of the display when operating in the record mode and data are read from the buffer memory when operating in the read mode. The buffer memory stores data for display and recording of it from the ELT screen. It is two units of 4,096 bytes each.

The YeS-7064 graphic display transmits data at a speed of 1,200-4,800 bits per second.

The working field of the display screen has dimensions of 250 X 250 mm.

The operator controls the device and exchanges information with the computer by means of an alphanumeric keyboard, functional keyboard and light pen (pencil).

The image on the screen is formed under the control of a program recorded in the buffer memory from the computer to which the device is connected through a standard integration channel of the YeS computer. The coordinates of points and vectors or character codes are arranged in the internal program of the device after the instruction that controls the operating mode of the device. A microfilming device can be used to produce a stable copy of the image on the screen.

8.5. External Storage Devices (VZU)

8.5.1. General Data

Memorization, storage and retrieval of a large volume of information is performed in computer systems designed to process economic information. External storage devices (VZU)--information stores--are used for this purpose. As was mentioned earlier, these devices include electromechanical VZU on magnetic tapes (NML), magnetic disks (NMD), magnetic drums (NMB) and magnetic cards (NMK). The operating principle of all these stores consists in the capability of ferromagnetic materials to be magnetized by a magnetic field and to retain residual magnetization for an unlimited time. The storage medium in magnetic storage devices is a layer of ferrolacquer or a galvanic coating.

The principle of recording information to a magnetic carrier and reading it from the carrier is identical for all magnetic carriers.

The basis of the magnetic recording process is interaction of a moving magnetic carrier and magnetic heads.

The magnetic head is a special electromagnet 1 (Figure 8.11), consisting of two half-rings and having an air gap 2 between the working surface of the carrier and the electromagnet.

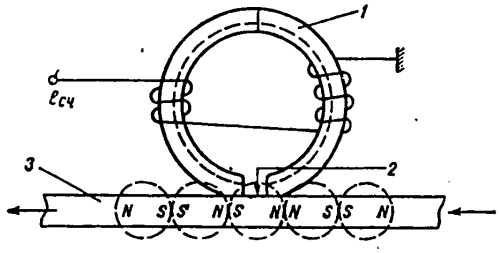

Figure 8.11. Principle of Magnetic Recording

Current pulses of different polarity are transmitted to the winding of the magnetic head to record information, as a result of which magnetic sections are formed on the carrier whose polarity corresponds to the numbers zero and one of the binary code.

The same heads, by means of which the recording is made, are usually employed to read information from the carrier surface. These heads are called universal.

When a carrier with magnetized sections passes under the head, EMF pulses (1_{sch}) having positive or negative signs, which correspond to zero and one codes, are excited in its winding.

Information is recorded on the magnetic carrier in parallel on several tracks, each of which has its own read/write head.

The main characteristics of VZU are storage capacity, speed and reliability. Storage capacity depends on the size of the carrier, the number of tracks and recording density and speed depends on the travel speed of the carrier. The characteristics of the carrier, the size of the gap between the carrier and the head and the method of recording affect the recording density.

All external storage devices are divided into those with sequential access to information and those with direct access. Sequential access devices include magnetic tape VZU and direct access devices include magnetic disk, magnetic drum and magnetic card VZU.

8.5.2. Magnetic Tape VZU

These devices are the most widespread high-capacity storage devices.

A tape 12.7 mm wide on which are located nine tracks, one of which (the fourth) is the verifying track--K (Figure 8.12), is used in modern computers (YeS EVM). Information is recorded and read by a unit consisting of nine record-read heads. One byte is recorded in one line on eight tracks in KOI-8 code. The information previously recorded on the tape is erased simultaneously with a new recording.

The method of recording without return to zero (NVN-1) and the phase-coded method (FK) are used in the storage devices. The first method is used to record with density of 8 and 32 bits/mm. In this case the method of recording ones is changing the state of the carrier magnetization and recording of zeros is the absence of variation of magnetization. With the second method zeros and ones are recorded with variation of the state of magnetization. This method is used for recording density of 63 bits/mm.

During recording, groups of bytes form a zone whose length is 18-2,048 bytes. With recording density of 32 bits/mm, a longitudinal verification line (PKS) and a cyclic verification line (TsKS) are recorded at the end of each zone. A cyclic verification line is recorded on the tape after the last byte of data with interval of 4 bytes. The longitudinal verification line is recorded after the cyclic verification line with interval of 4 bytes. With recording density of 8 and 63 bits/mm, only the PKS is recorded at the end of the zone. The interzone intervals

are used for starting and stopping the tape. Their minimum length is 12.7 mm and nominal length is 15.2 mm. The maximum length of the tape in the reel is 750 meters.

Beginning of tape (NL) and end of tape (KL) markers, recognized during rewinding of the tape by the photoelectric method, are glued at a distance of 3-5 meters from the beginning and end of the tape. The signals transmitted by the sensors warn of the approach of the end of tape. Information is recorded on the tape, beginning from the NL marker and recording ends 3 meters after the KL marker.

Vertical redundancy verification (vertical verification) and horizontal redundancy verification (horizontal verification) and also verification using a cyclic code (cyclic verification) are used to verify the correctness of the information recorded and read.

Vertical verification is used to verify the number of single bits for oddness along the vertical and longitudinal verification is used to check the number of single bits for oddness along each track of a separate zone. If an even number of single bits is detected in the byte by the comparison circuit, an error is recorded.

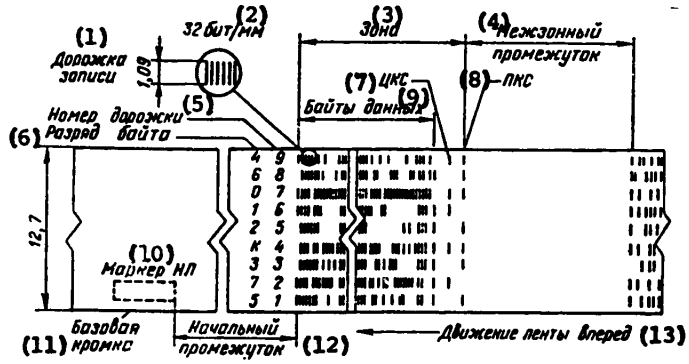

Figure 8.12. Recording of Information on Magnetic Tape by the YeS Computer with Recording Density of 32 Bits/mm

Key:

1. Recording track
2. 32 bits/mm
3. Zone
4. Interzone interval
5. Number of track
6. Digit of byte
7. Cyclic verification line
8. Longitudinal verification line
9. Data bytes
10. Beginning of tape marker
11. Base edge
12. Initial interval
13. Forward movement of tape

Cyclic verification consists in the fact that a verification byte, which is recorded on the tape after the last data byte and before the longitudinal verification byte, is calculated in the control device by means of a cyclic code. During readout, this byte is again calculated and compared to that recorded on the tape.

If there is incongruence, the control device emits an error signal. Cyclic verification is carried out only on tapes having recording density of 32 bits/mm. This type of verification is not used with the phase-coded method. The maximum amount of information which can be located on a single reel of magnetic tape 750 meters long with longitudinal recording density of 8 bits/mm is approximately 5.5 Mbytes, with recording density of 32 bits/mm is 22 Mbytes and with recording density of 63 bits/mm is 44 Mbytes.

Storage devices are connected to the input-output channels of the computer by means of storage control devices. These devices have two operating modes--autonomous and channel-operating mode. Switching from one mode to another is carried out from the control console. The device is checked and adjusted in the autonomous mode by means of a control console and display console.

Various types of magnetic tape storage devices--YeS-5010, YeS-5012, YeS-5014, YeS-5016 and so on--are used in models of the YeS computers. Their specifications are presented in Table 8.4.

8.5.3. Magnetic Disk External Storage Devices (NMD)

Magnetic disk external storage devices are related to those with direct access and are storage devices in which the storage medium is a magnetic film. These VZU have large capacity and relatively short access time. The capacity of magnetic disk stores in modern models of computers reaches hundreds and thousands of millions of bits, while the read/write speed reaches up to one million bits per second.

Let us consider the general principles of NMD design. A magnetic disk is usually manufactured of aluminum with a ferromagnetic coating 250-650 mm in diameter and 2.0-2.5 thick. A ferromagnetic coating is applied to both sides of the disk. Information is recorded in concentric tracks of the disk. Each side of the disk is divided into zones to reduce the track retrieval time. Disks attached to the same axis are called a pack. A disk pack may be interchangeable or stationary (permanent). In this regard storage devices are divided into two groups--interchangeable magnetic disk stores (NSMD) and permanent magnetic disk stores (NPMD). A pack may contain a different number of disks--from four to several tens. A pack consists of six disks with 10 working surfaces (the upper and lower disks have one each working surface) in interchangeable disk stores of the YeS computers.

The disk unit is divided into two units of 18 disks each in permanent magnetic disk stores (YeS-5051). The total number of working surfaces in these stores is 64.

Information is recorded on the track sequentially bit by bit in all magnetic disk stores. The numbers of the tracks are counted from the edge of the magnetic disk. Part of the tracks in NMD is allocated as reserve tracks for use in case flaws are detected in the other tracks. Tracks with identical numbers form a cylinder. The number of tracks in a cylinder is equal to the number of working surfaces of the pack.

There is a mechanism for access to the read/write heads, which is a lever unit by means of which the heads are set to any track of the working surface of the disks,

Table 8.4. Main Specification of Magnetic Tape Stores of YeS Computers

(1) Технические характеристики / (2) Устройства	(3) EC-5010 (СССР)	(4) EC-5012 (НРБ)	(5) EC-5014 (СССР)	(6) EC-5015 (ЧССР)	(7) EC-5016 (ГДР)	(8) EC-5017 (СССР)	(9) EC-5019 (ПНР)	(10) EC-5022 (ЧССР)	(11) EC-5025 (СССР)	(12) EC-5503 (СССР)
(13) Скорость движения ленты, м/с	2	2	2	4	1,5	2	3	4	2	5
(14) Скорость перемотки ленты, м/с	2	2	5	8,5	3	5	5	8,5	5	18
(15) Плотность записи, бит/мм	8; 32	8; 32	63	63	32	8; 32	8; 22; 32	8; 32	32; 63	32; 63
(16) Скорость передачи данных, Кбайт/с	64	64	126	252	48	64	30; 82; 120	126	126	315
(17) Номинальный межзоновый промежуток, мм	15,2	15,2	15,2	15,2	15,2	15,2	15,2	15,2	15,2	15,2
(18) Длина ленты, м	750	750	750	750	750	750	750	750	750	750
(19) Ширина ленты, мм	12,7	12,7	12,7	12,7	12,7	12,7	12,7	12,7	12,7	12,7
(20) Код устройства управления (21)	EC-5511	EC-5512	EC-5514	EC-5515	EC-5516	EC-5517	EC-5519	EC-5515	EC-5525	EC-5503

Key:

1. Specifications
2. Devices
3. YeS-5010 (USSR)
4. YeS-5012 (Peoples Republic of Bulgaria)
5. YeS-5014 (USSR)
6. YeS-5015 (CSSR)
7. YeS-5016 (GDR)
8. YeS-5017 (USSR)
9. YeS-5019 (Polish Peoples Republic)
10. Yes-5022 (CSSR)
11. YeS-5025 (USSR)
12. YeS-5503 (USSR)
13. Tape speed, m/s
14. Tape rewinding speed, m/s
15. Recording density, bits/mm
16. Data transmission speed, Kbytes/s
17. Nominal interzone interval, mm
18. Tape length, meters
19. Tape width, mm
20. Code of control device
21. YeS

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for access to the tracks on each storage device. Interchangeable disks of the YeS computers have recording density of 30 bits/mm on the outside track and 44 bits/mm on the inside track.

A functional diagram of a magnetic disk storage device is shown in Figure 8.13. Magnetic disks 1 rotate on a drive shaft 6 at a speed of 1,000-3,000 rpm. Spring levers 2 with magnetic heads 3 are located between the disks. The levers are rigidly attached to a carriage 4, which can move along a guide shaft 5. The magnetic heads move along the radius of the disks within their own zone 7.

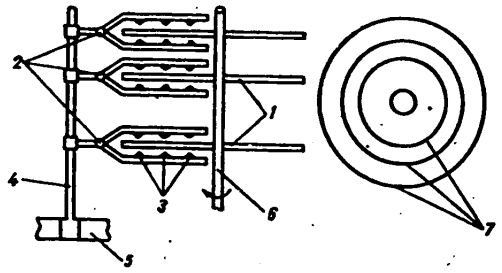

Figure 8.13. Functional Diagram of Magnetic Disk Storage Device

A diagram of the interaction of the magnetic heads and the YeS-5053 interchangeable magnetic disk pack is shown in Figure 8.14. This pack consists of six disks whose outer diameter is equal to 336.4 mm. The surface of the disks is coated with ferrolacquer 4-5 microns thick.

Working disks have a thickness of 1.27 mm. The distance between the disk surfaces is 10.16 mm. The YeS-5053 pack permits recording on 200 main and three reserve tracks on each surface of the disk. Tracks with addresses 200, 201 and 202 are used as reserve tracks. The track with address 073 is regarded as the verification track. A total of 3,625 bytes can be recorded on a single track. Ten tracks arranged one under the other on 10 working surfaces of the disks form a cylinder. The capacity of a single cylinder is 36,250 bytes while the capacity of the total pack is 7.25 Mbytes. The disk pack rotates in the storage device at a speed of 2,400 rpm.

The storage device has 10 universal magnetic read/write heads (one head each on each working surface) and 10 erase heads arranged in a single housing for writing and reading information.

Only one of 10 heads operates simultaneously when writing or reading information. They write (read) information on the same track digit by digit.

The heads are numbered from bottom to top from 0 to 9. The address of each track in the pack is determined by the cylinder address and the number of the head.

The time recorded to retrieve and transmit data consists of the cylinder retrieval time, head selection time, carrier rotation delay time and data transmission time. The total time of the indicated components is called access time.

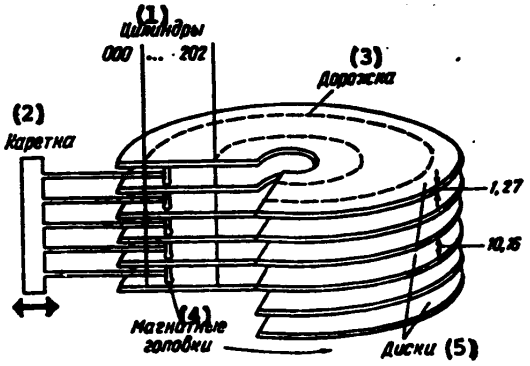

Figure 8.14. Diagram of Interaction of Magnetic Heads and YeS-5053 Magnetic Disk Pack

Key:
1. Cylinders
2. Carriage
3. Track
4. Magnetic heads
5. Disks

The erase head is arranged behind the read/write head in the direction of rotation of the disk. During data recording, this head demagnetizes the intervals between adjacent tracks, which reduces the mutual interference from these tracks during subsequent reading of information.

The YeS-5050, YeS-5052, YeS-5055, YeS-5056 and YeS-5058 magnetic disk stores operate with interchangeable magnetic disk packs of type YeS-5053. These stores have identical main specifications, namely: capacity of 7.25 Mbytes and data transmission speed during writing and reading of 156 Kbytes/s. They are distinguished mainly by the average access time (see Table 8.5).

The YeS-5061 NMD, which operates with YeS-5261 interchangeable disk pack, has a significant difference. The YeS-5261 pack differs from the YeS-5053 pack by the fact that it contains 11 rather 6 disks (20 working surfaces) while each cylinder contains 20 tracks. Recording density is 60 bits/mm on the outside track and 90 bits/mm on the inside track, which permits recording of 7,250 bytes on a single track. The capacity of the pack is 29.17 Mbytes and data transmission speed is 312 Kbytes/s.

The most productive interchangeable magnetic disk store is the YeS-5066, in which a pack of 12 YeS-5266 disks is used. Recording is accomplished on 19 surfaces of the disks. There are 404 main and 7 reserve tracks on each surface. A total of 13,030 bytes is recorded on each track with recording density of 160 bits/mm. The pack capacity comprises 100 Mbytes. The data transmission speed is 806 Kbytes/s.

Permanent magnetic disk stores include the YeS-5051 (USSR) and YeS-5060 (Hungarian Peoples Republic).

Table 8.5. Main Characteristics of Magnetic Disk Stores of YeS Computers

(1) Технические характеристики	(2) Устройства	(3) ЕС-5050 (СССР)	(4) ЕС-5051 (СССР)	(5) ЕС-5052 (НРБ)	(6) ЕС-5055 (ГДР)	(7) ЕС-5056 (СССР)	(8) ЕС-5058 (ЧССР)	(9) ЕС-5061 (НРБ)	(10) ЕС-5060 (ВНР)	(11) ЕС-5066 (НРБ)
Тип накопителя (12)		НСМД (13)	НПМД (14)	НСМД	НСМД	НСМД	НСМД	НСМД	НПМД	НСМД
Емкость, Мбайт (15)		7,25	125	7,25	7,25	7,25	7,25	29,17	0,8	100
Количество рабочих цилиндров (16)		200	384	200	200	200	200	200	256	404
Количество дорожек в цилиндре (17)		10	1	10	10	10	10	20	1	19
Количество подключаемых каналов (18)		2	2	2	1	2	1	2	—	2
Среднее время доступа, мс (19)		90	250	60	90	90	110	50	10	32
Скорость передачи данных, Кбайт/с (20)		156	83,25	156	156	156	156	312	150	806
Код устройства управления (21)		EC-5551 (22)	EC-5551	EC-5552	EC-5555	EC-5551	EC-5558	EC-5561	—	EC-5566

Key:

1. Specifications
2. Devices
3. YeS-5050 (USSR)
4. YeS-5051 (USSR)
5. YeS-5052 (Peoples Republic of Bulgaria)
6. YeS-5055 (GDR)
7. YeS-5056 (USSR)
8. YeS-5058 (CSSR)
9. YeS-5061 (Peoples Republic of Bulgaria)
10. YeS-5060 (Hungarian Peoples Republic)
11. YeS-5066 (Peoples Republic of Bulgaria)
12. Type of storage device
13. Interchangeable magnetic disk store
14. Permanent magnetic disk store
15. Capacity, Mbytes
16. Number of working cylinders
17. Number of tracks in cylinder
18. Number of switchable channels
19. Average access time, ms
20. Data transmission speed, Kbytes/s
21. Code of control device
22. YeS

The YeS-5051 store has a permanent magnetic disk pack divided into two units of 18 disks each. Storage capacity is 125 Mbytes, the number of working heads is 192 and the average access time is 250 ms.

The YeS-5060 store has a single magnetic disk with fixed heads. It is designed to work with the YeS-1010 computer. The outer diameter of the disk is 317 mm and thickness is 9 mm. Disk rotation speed is 3,600 rpm. A total of 17 magnetic head units, in each of which there are 16 working and one reserve head, are arranged on both sides of the disk in the store. Recording density is 40 bits/mm. Disk capacity is 800 Kbytes and information exchange speed is 150 Kbytes/s.

The specifications of magnetic disk stores used in models of the YeS computers are presented in Table 8.5.

An identical track format (Figure 8.15), which is determined by the control device, is used in models of the YeS computers. There are sections on the disk tracks for recording operating and control information. Control information is used to organize and verify direct access and contains track and recording addresses, length of recording and intervals between zones.

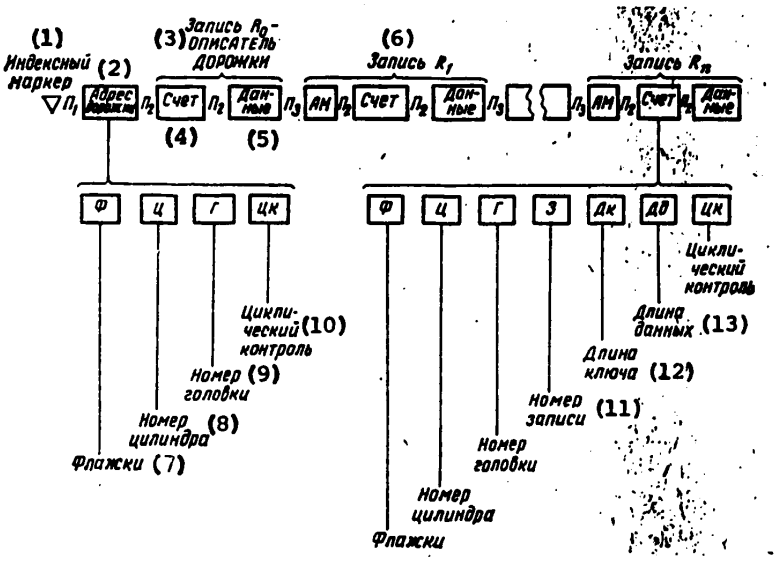

Figure 8.15. Recording Information on Magnetic Disks of "Counting-Data" Format

Key:

1. Index marker
2. Track address
3. Recording R_0-TRACK DESCRIBER
4. Counting
5. Data
6. Record

[Key continued on following page]

[Key continued from preceding page]:

7. Flags
8. Cylinder number
9. Head number
10. Cyclic verification
11. Number of recording
12. Key length
13. Length of data

The beginning of all tracks on the working surface of the disk is noted with an index marker. The first recording on the track is its address. An address consists of seven bytes--one features byte, which indicates the status and use of the track (working, defect, main and reserve), four address bytes that indicate the numbers of the cylinder and head and two cyclic verification bytes. The intervals are bytes which are recorded by the control device to delineate the recording zones. Intervals P_1 and P_2 have constant length for each of the types of storage devices and the length of interval P_3 depends on the length of the previous recording.

Recording (track describer) with zero ordinal number (R_0) is placed on the track after the track address. The length of this recording is equal to 8 bytes and contains information of the control program.

The information records of the user are placed on the track after R_0. In this case the address marker (AM) is initially recorded and then the physical recordings of formats--"counting-data" or "counting-key-data"--are recorded.

The counting zone contains 11 bytes and includes the following fields--features (1 byte), recording identifier (5 bytes), key length (1 byte), data length (2 bytes) and cyclic verification (2 bytes).

8.5.4. Magnetic Drum External Storage Devices (NMB)

The magnetic drum is a hollow cylinder, 320-630 mm in diameter and 400-700 mm long, manufactured from dimagnetic material with a thin layer of ferromagnetic coating up to 40 microns thick. The layer applied to the surface of the drum acts as a magnetic carrier. Magnetic heads, which are arranged along the generatrix of the drum (Figure 8.16), serve to record information on the drum.

The drum is set into rotation by an electric motor at a constant speed. Upon rotation of the drum, the magnetic heads create a magnetic field which is used to record information. The heads record on tracks arranged around the circumference of the drum. The gap between the heads and the surface of the drum is 20-50 microns. Recording density is equal to 4-8 bits/mm. Movable heads automatically shifted to the necessary track are used in high-capacity drums.

The capacity of the storage device is determined by the drum dimensions, number of heads and information recording density. In modern computers magnetic drum storage devices have a capacity of 5,000-400,000 bits. The average access time to any section of the drum surface is the time expended on a half revolution of the drum. The magnetic heads are usually arranged in two units. A YeS-5033 (USSR) and YeS-5035 (Peoples Republic of Bulgaria) type NMB is used in YeS computers.

There are eight read/write heads for each addressable track in the YeS-5033 storage device. The YeS-5033 has diameter of 450 mm, capacity of 6 Mbytes, 800 tracks on which information is recorded with density of 50 bits/mm, data transmission speed of 1,250 Kbytes/s and drum rotation speed of 1,500 rpm.

The YeS-5033 storage device can be regarded as a single cylinder consisting of 100 addressable tracks. There are eight write/read heads for each addressable track. The YeS-5033 is used in older models of the Unified Computer System: YeS-1040, YeS-1050 and YeS-1060.

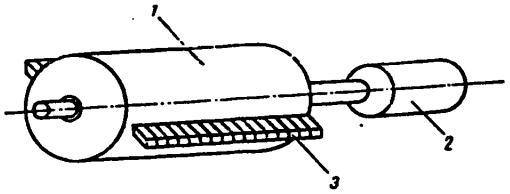

Figure 8.16. Magnetic Drum: 1--magnetic drum; 2--electric motor; 3--magnetic heads

The YeS-5035 storage device has the following specifications: capacity of 2 Mbytes, number of tracks per drum of 532, recording density of 33.5 bits/mm, data transmission speed 100 Kbytes/s and drum rotational speed of 1,500 rpm.

Information can be recorded in magnetic drum storage devices by three methods; series, parallel and parallel-series.

With the series method all digits of a number are arranged along a single track of the drum; with the parallel method each digit of the number is arranged on an individual track and with series-parallel the number is divided into groups which are written on the drum sequentially. The most widespread method is the parallel-series.

Magnetic drum storage devices, like magnetic disk storage devices, are related to direct access stores.

The advantages of magnetic drum storage devices are large capacity, simple access, capability of multiple reading and servicing convenience. The disadvantages are sequential selection and mechanical rotational movement in which the gap between the magnetic heads and the surface of the drum is retained.

The latest models of interchangeable magnetic disk storage devices, YeS-5061 and YeS-5066, are essentially not inferior in speed to magnetic drum storage devices, but they considerably exceed them in capacity and provide rapid replacement of the information carrier.

8.5.5. Magnetic Card External Storage Devices

The YeS-5071 magnetic card storage device is designed to write, store and read large information files (up to 10^9 bits). It is used together with the YeS-5551 control device in YeS-1020, YeS-1030 and YeS-1050 models.

The YeS-5071 storage device consists of an intermediate control device and storage device. The intermediate control device provides communiation of the main YeS-5551 control device with the storage device. It is designed to control information writing/reading on magnetic cards, information encoding (decoding) and error checking.

The storage device is used to store magnetic cards, to move them to the read/write heads and to transmit the read information to the control device. It consists of an automatic card file unit (BAK), automatic card file control (BUAK), card feed unit (BKM) and engineer's console. There is a magazine in the automatic card file unit to store 512 groups of cards consisting of two sections. Up to 32 containers are included in the sections. A group of cards is removed from the selected container and it is transmitted to the card feed unit by a special hoist. Cards are selected sequentially from a selected group and information is also written and read in the card feed unit.

The engineer's console is equipped with manual control devices to check the storage device and also for manual replacement of card groups in the card file.

The YeS-5071 storage device has the following specifications: capacity of 125 Mbytes, recording density of 32 bits/mm, read/write speed of 52 Kbytes/s, average information access time of 5,000 ms, capacity of one magnetic card of 2,048 bytes, (16 + 4) tracks on a card, hopper capacity of 128 cards and number of hoppers in storage device of 512.

Comparative analysis of the main engineering and functional parameters of a magnetic tape and direct access storage devices shows that they have approximately identical capacity and information exchange speed during writing and reading. The advantage of the direct access storage device is undoubtedly the short information retrieval time and the cost of storing a unit of information on magnetic disks, drums and magnetic cards is approximately an order higher than storing it on magnetic tapes. Therefore, these features of storage devices should be taken into account when operating them in computer systems.

Chapter 13. User Station System

13.1. General Data

User access to computers is gained in TD [Remote data processing] systems mainly through user stations (AP). User stations are peripheral computer devices installed outside the machine room and connected to communications lines. If a user station contains equipment for manual input of information, it is designated mainly for information gathering and if the user station contains a display with keyboard it is used to work in the dialogue mode. Moreover, a user terminal can

be used autonomously as a data preparation device. It may also include teletypes, automatic devices connected to machine tools and various installations and so on. But in all cases the user station is the connecting link between the computer and its users.

Information can be prepared and transmitted in a user station in the on-line mode when data are fed directly from devices, keyboards and documents to the communications channel for transmission to the computer or in the off-line mode when data are initially recorded on magnetic tapes, punch cards and papertapes and then are entered from these carriers. In this case the user station is equipped with the corresponding input devices.

The output data fed from the computer to the user terminal can also either directly control specific production processes or be led to intermediate carriers (user stations are equipped with punch card and papertape output devices) and for printout (user stations are equipped with typewriters and printers).

All the user station equipment is connected to the control device, which is a compulsory component of a user station and which performs the following basic functions:

establishment and breaking of communications with the MPD [Data transmission multiplexer];

data conversion from transmission code to the code fo the external device when receiving information from the computer;

reverse conversions when transmitting information from the user station to the computer;

calculation and comparison of check sums when transmitting information in blocks;

matching input-output and information transmission speeds;

provision of autonomous and operating modes of functioning of the input-output devices and so on.

Besides the control device, the user station also contains terminal devices. Unlike local terminals connected directly to the computer, the terminals installed at user stations are called remote terminals. Alphanumeric terminals (teletype and typewriter), graph terminals (graph plotters, ELT with graph input) and so on may be used in user stations.

Transfer functions are accomplishedby the UPS [Signal shaping device] and modems built into the user station.

From the viewpoint of users, user stations should meet the following basic requirements:

the capability of the user working in practically any high-level algorithmic language;

simplicity of working with the system, especially for personnel who are not regular users. The communication language for this interaction should be close to natural language and the equipment used should be simple to operate.

accessibility, i.e., the capability of rapid connection of the user to the system at any time;

a developed checking system that ensures high reliability of data transmission;

short answer waiting time;

prevention of unsanctioned access to unauthorized personnel.

User stations differ from each other by the types of communications channels, the data transmission modes and methods, the area of appliation and types of installed terminal devices.

Thus, for example, user stations may provide information exchange with the computer in the dialogue mode when the data are usually entered directly into the computer from a keyboard and in the batch transmission mode. In this case the data are first prepared, partially processed and are then transmitted to the computer. Most user stations can operate in these two modes.

If the user station is not connected permanently to the remote data processing system and requires that connection establishment procedures which are performed by automatic output and answering devices, then the capability of connection both from the computer and from the user station is determined by procedures of the competition mode. When several user stations are connected to the same allocated line, an additional change of control procedure is required to select the type of user station which should transmit or receive data. To do this, the subordination mode is used, which is characterized by the determining role of the computer in the communications establishment procedure.

Depending on the number of operators working simultaneously, user stations can be individual and group use type. Group user stations always have a large number of input-output devices and also a storage device consisting of functionally independent units whose number corresponds to the number of users.

The following are distinguished depending on the equipment being used:

collective and individual user stations in which part of the work is performed by minicomputers contained in them. These user stations can be used in all operating modes; transmission speed is 9,600 bauds and reliability is 10^{-9}. An example of this user station may be the AP-50, related to the remote data processing system of the YeS computers;

user stations equipped with papertape and punch card input-output devices, alphanumeric printers and magnetic tape storage devices. The batch processing

mode, high speeds (up to 4,800 bauds) and transmission reliability are characteristic of these user stations. The given type of user stations includes, for example, the AP-4 of the remote data processing system of the Unified Computer System;

a user station with one or several visual information display devices. Alphanumeric display user stations, consisting of ELT display devices, a keyboard and printer, are most widely used in computer networks. Their advantages are high rate of information exchange with the computer, capability of editing data and so on. These user stations (these are the AP-61, AP-62 and so on in the remote data processing system of the unified computer system) are used mainly in the dialogue mode;

user stations having input-output devices with keyboard. This type of user station is rather widespread since it is simple to service and does not place high requirements either on speed or the reliability of transmission. The remote data processing system of the unified computer system offers several types of these user stations: AP-2, AP-3, AP-70 and so on;

user stations in which teletypes, characterized by low cost and simple operation, are installed. However, the transmission speed in them usually does not exceed 200 bauds;

user stations in which there is equipment used to connect monitoring and measuring devices, recording devices, preliminary information gathering and recording devices, bookkeeping equipment and so on. These user stations (for example, the AP-5 and AP-6 in the remote data processing system of the unified computer system) operate in real time and have rather high speed.

Besides the considered user stations, programmable user stations have been developed and used which can partially process information independently of a central computer. These user stations contain a processor, internal storage and operating system.

User stations are used in the most diverse areas. Thus, for example, user stations that gather data and accomplish real-time control are used extensively in different ASU [Automated control system]. Systems have already been developed in which data is gathered from sensors or measuring devices by means of terminals. The gathered data are fed over communications lines to networks for subsequent transmission and processing. For real-time control, user stations include either a buffer storage or a small computer, sensors, real-time clocks, measuring devices, analog-digital converters and so on. The aggregate of these devices is used to observe and correct high-speed processes and also to transmit and process the received information.

Terminals are used for manufacturing and commercial services mainly in user stations that gather data in manufacturing operations or product output at production enterprises and also for gathering data on the exchange of goods sold at department stores and self-service stores. These terminals have built-in data checking or refining devices, automatic devices for reading encoded marks or tags on goods or produced products.

User stations operating in the dialogue mode have the highest speeds in remote data processing systems. For these purposes the user stations are equipped either with electric typewriters or with alphanumeric or graphic displays. The main disadvantage of using these user stations is the absence of copies of the output results.

The composition of a user station is determined as a function of the volumes of information, the type of user problems solved, the information exchange rate and many other factors.

13.2. User Stations of the Remote Data Processing System of the Unified Computer System

User stations of the remote data processing system of the unified computer system contain a wide range of external devices that gather and transmit data, display it on a display screen, enter tasks into the computer, make inquiries and issue lists, monitor and manage production and so on. Besides external devices, user stations of the unified computer system are distinguished from each other by the type of communications channels used, the type of connected data transmission multiplexers and some other characteristics. The basic data on user stations, related to the remote data processing system of the unified computer system, are presented in Table 13.1.

The characteristic feature of the AP-1 user station (YeS-8501) is the presence of papertape and edge-perforated punch card input-output devices, a typewriter, buffer storage with capacity of 160 characters, control unit, telephone apparatus and so on in it. All this equipment ensures semiduplex data exchange over commutated and segregated telephone and uncommutated telegraph communications channels at a transmission speed up to 1,200 bauds.

When operating in the autonomous mde, the AP-1 types information on a typewriter with simtulaneous preparation of papertapes and edge-perforated punch cards, prints out data entered earlier on the papertape and reperforates the tape.

The capability of connection to any data transmission multiplexer, the presence of various external devices and the variety of functions performed contribute to the extensive use of the AP-1 in remote data processing systems for data gathering, inquiry processing and so on.

The AP-2 user station (YeS-8502) also includes papertape and edge-perforated punch card input-output devices, a Konsul-260.1 typewriter (YeS-7172), a modem-200 and so on. The AP-2 has two models differing by exchange algorithms and the type of data transmission multiplexers: one model is connected to the MPD-3 and the second is connected to the MPD-1A and MPD-2. Both models operate at a speed of 200 bauds. One of the possible configurations of the remote data processing system of the unified computer system using the AP-2 is presented in Figure 13.1.

All the enumerated user stations are designed to transmit data in the pack mode. The AP-4 user station (YeS-8504) provides the dialogue mode. It can be equipped with papertape and punch card input-output devices, alphanumeric printers, magnetic tape store and a typewriter. A single user station can contain no more than eight of any external devices installed at a distance up to 500 meters from

Table 13.1. Specifications of User Stations

(1) Модель	(2) Код	(3) Страна-изготовитель	(4) Состав АП: (5) устройство ввода с перфолент и перфокарт с краевой перфорацией	(6) устройство ввода с перфолент	(7) устройство ввода с перфокарт	(8) устройство вывода на перфоленты и перфокарты с краевой перфорацией	(9) устройство вывода на перфоленты	(10) устройство вывода на перфокарты	(11) дисплей	(12) АЦПУ	(13) пишущая машинка	(14) НМЛ	(15) перфожетоны, перфопаспорт	(16) Вид канала связи	(17) Скорость передачи, бод	(18) Вид МПД
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
АП-1 (19)	(20) ЕС-8501	(21) НРБ	+			+					+			(22) Коммутируемый и выделенный телефонный, некоммутируемый телеграфный	50, 75, 100, 200	(23) Все МПД
АП-2	ЕС-8502	(24) Вариант 1 ВНР	+			+					+			То же (22)	200	МПД-3
	(25)	Вариант 2 СССР	+			+					+			»	200	МПД-2, МПД-1А
АП-3	ЕС-8503	НРБ (21)		+			+				+			(26) Коммутируемый и выделенный телефонный	600, 1 200	МПД-3
АП-4	ЕС-8504	(27) СССР		+	+		+			+	+	+	(28)	Выделенный телефонный	600, 1 200, 2 400	МПД-1А, МПД-2, МПД-3
АП-5	ЕС-8505	(29) ГДР		+	+		+			+	+		+	То же (28)	200, 600, 1 200	МПД-4
АП-6	ЕС-8506	ГДР		+	+		+				+		+	»	600, 1 200	МПД-4

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Table 13.1 (Continued).

Модель АП	Код	Страна-изготовитель	Состав АП: устройство ввода с перфоленты и перфокарт с краевой перфорацией	устройство ввода с перфоленты	устройство ввода с перфокарт	устройство вывода на перфоленты и перфокарты с краевой перфорацией	устройство вывода на перфоленты	устройство вывода на перфокарты	Диспей	АЦПУ	пишущая машинка	НМЛ	перфоленточн. перфонакопт	Вид канала связи	Скорость передачи, бод	Вид МПД
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
АП-11	ЕС-8511	СССР		+	+	-	+	+	+	+	+		(28)	Выделенный телефонный	600, 1 200, 2 400	МПД-2, МПД-1А
АП-14	ЕС-8514	ПНР (30)		+	+		+		+	+	+	+	(26)	Коммутируемый и выделенный телефонный	600, 1 200, 2 400	МПД-1А, МПД-2, МПД-3
АП-31	ЕС-8531	НРБ	+	+	+	+	+				+	+		То же	200, 600, 1 200	МПД-1, МПД-1А, МПД-2, МПД-3
АП-32	ЕС-8532	ГДР		+	+		+				+	+		»	200, 600, 1 200	МПД-1А, МПД-2,- МПД-3, МПД-4
АП-50	ЕС-8550	ВНР (31)		+	+		+		+	+	+	+		»	600, 1 200, 2 400, 4 800, 9 600	МПД-1А, МПД-2, МПД-3
АП-61	ЕС-8561	СССР							+		+	+		Выделенный телефонный	600, 1 200, 2 400	МПД-1, МПД-1А, МПД-2, МПД-4
АП-62	ЕС-8562	ВНР							+		+	+		Выделенный телефонный	200, 600, 1 200, 2 400	МПД-1, МПД-1А, МПД-2, МПД-4
АП-63	ЕС-8563	СССР							+		+	+		Выделенный телефонный	600, 1 200, 2 400	МПД-1, МПД-1А, МПД-2, МПД-4
АП-64	ЕС-8564	ВНР							+		+	+		То же	600, 1 200, 2 400, 4 800	МПД-1, МПД-1А, МПД-2, МПД-4

[Continued on following page]

Table 13.1 (Continued).

Модель	Код	Страна-изготовитель	Состав АП: устройство ввода с перфолент и перфокарт с кареткой перфопечати	устройство ввода с перфолент	устройство ввода с перфокарт	устройство ввода из перфолент и перфокарт с кареткой перфопечати	устройство вывода на перфоленты	устройство вывода на перфокарты	Диспей	АЦПУ	вишущая машинка	НМЛ	перфоленточн. перфонаситор	Вид канала связи	Скорость передачи, бод	Вид МПД
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
АП-70	ЕС-8570	СССР, НРБ (33)									+		(34)	Коммутируемый и выделенный телефонный, выделенный телеграфный	100	Все МПД
(35) Телеграфный аппарат пятиэлементного кода	ЕС-8591, ЕС-8592	(36) ЧССР, ГДР											(37)	Коммутируемый и выделенный телеграфный	50, 75, 100	МПД-1, МПД-1А, МПД-2, МПД-3
Телеграфный аппарат семиэлементного кода	ЕС-8593	ЧССР												(37) То же	100, 200	МПД-1, МПД-1А, МПД-2, МПД-3

Key:

1. Model
2. Code
3. Manufacturing country
4. Composition of user station
5. Papertape and edge-perforated punch input device
6. Papertape input device
7. Punch card input device
8. Papertape and edge-perforated punch card output device
9. Papertape output device
10. Punch card output device

[Key continued on following page]

[Key continued from following page]:

11. Display
12. Alphanumeric printer
13. Typewriter
14. Magnetic tape store
15. Punched badges and punched nameplates
16. Type of communications channel
17. Transmission speed, bauds
18. Type of data transmission multiplexer
19. AP
20. YeS
21. Peoples Republic of Bulgaria
22. Commutated and segregated telephone and uncommutated telegraph
23. All MPD
24. Version 1, Hungarian Peoples Republic
25. Version 2, USSR
26. Commutated and segretated telephone
27. USSR
28. Segregated telephone
29. German Democratic Republic
30. Polish Peoples Republic
31. Hungarian Peoples Republic
32. Segregated telephone and telegraph
33. USSR and Bulgarian Peoples Republic
34. Commutated and segregated telephone and segregated telegraph
35. Telegraph apparatus of five-element code
36. CSSR and German Democratic Republic
37. Commutated and segregated telegraph
38. Telegraph apparatus of seven-element code

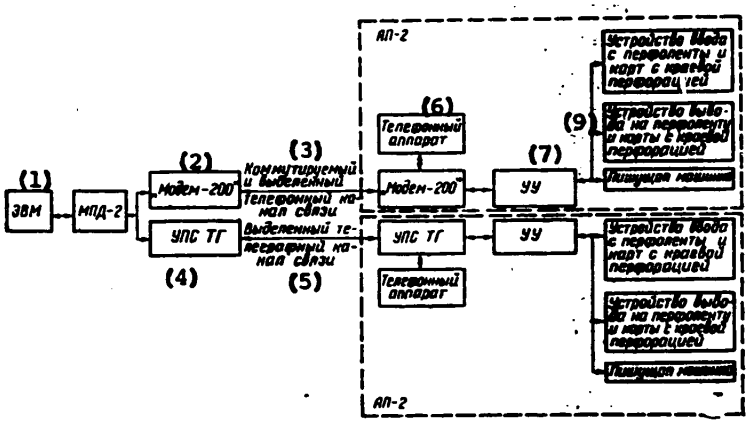

Figure 13.1. Configuration of Remote Data Processing System of Unified Computer System Using AP-2 (Model 2)

[Key on following page]

[Key continued from preceding page]:

1. Computer
2. Modem-200
3. Commutated and segregated telephone communications channel
4. Telegraph signal conversion device
5. Segregated telegraph communications channel
6. Telephone apparatus
7. Control device
8. Papertape and edge-perforated punch card input device
9. Papertape and edge-perforated punch card output device
10. Typewriter

the control unit (Figure 13.2). The AP-4 also has a memory with capacity of 32 Kbytes and an operating system. It operates only on commutated communications channels through a modem-1200 at a speed of 600, 1,200 and 2,400 bauds and is connected to the MPD-1A, MPD-2 and MPD-3.

The main designation of the AP-5 user station (YeS-8505) is data gathering and also producting monitoring and control. In this regard it can be equipped at the desire of users with papertape input-output devices and up to 15 peripheral devices that connect the inquiry read device from punched badges and punched nameplates, an alphanumeric keyboard, inquiry device of measured value sensors, printer and so on. The SP-5 operates over uncommutated telegraph communications channels at a speed of 200, 600 and 1,200 bauds and is connected to the MPD-4

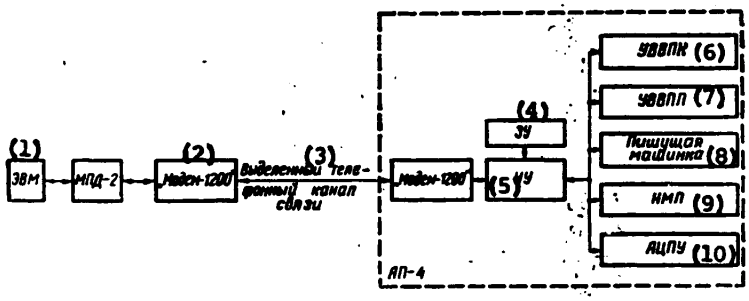

Figure 13.2. Configuration of Remote Data Processing System of Unified Computer System Using AP-4

Key:

1. Computer
2. Modem-1200
3. Segregated telephone communications channel
4. Storage device
5. Control unit
6. Punch card input-output device
7. Papertape input-output device
8. Typewriter
9. Magnetic tape store
10. Alphanumeric printer

The characteristics of the AP-5 coincide almost completely with similar parameters of the AP-6 user station (YeS-8506). The main differences include broader composition of external devices of the AP-6, greater amount of connected equipment and the presence of a programming device having up to 16 different programs.

The AP-11 user station (YeS-8511), which provides semiduplex data exchange mode over segregated telephone channels at a transmission speed of 1,200 and 2,400 bauds, includes punch card and papertape input-output devices, a Konsul-260.1 typewriter, alphanumeric printer and modem-2400. The AP-11 communicates with the computer through the MPD-1A and MPD-2.

The AP-14 user station (YeS-8514), equipped with papertape input-output devices, punch card input device, alphanumeric printer, magnetic tape store, display, typewriter and so on, can be used both in dialogue remote data processing systems and in batch transmission systems. The makeup of the AP-14 may be variable. Transmission is accomplished over commutated and segregated telephone communications channels through a modem-1200 and modem-2400.

The AP-31 (YeS-8531) and AP-32 (YeS-8532) user stations consist of punch card and papertape devices, magnetic tape store (AP-31) and equipment that uses edge-perforated cards (AP-32). The transmission speed over telephone channels is 200, 600 and 1,200 bauds.

The AP-50 user station (YeS-8550) was developed on the basis of the YeS-1010 minicomputer and transmits over commutated and segregated telephone communications channels at a speed of 600, 1,200, 2,400, 4,800 and 9,600 bauds. The AP-50 is connected to the computer through an MPD-1A, MPD-2 and MPD-3.

The AP-61 (YeS-8561) and AP-62 (YeS-8562) user stations were constructed on the base of a visual display, by means of which information is exchanged operationally in the dialogue mode through all types of data transmission multiplexers, except the MPD-3. The AP-61 and AP-62 provide semiduplex communications over segregated telephone channels at a speed of 1,200 and 2,400 bauds. The AP-62 can also operate over segregated telegraph communications channels.

The main devices of these user stations are:

cathode-ray tube (ELT) display measuring 35 cm in the diagonal. The working field of the ELT screen permits display of 960 characters. The method of printing the characters is point;

an alphanumeric keyboard located separately from the display has 28 keys to control the entered information, edit and print it, and also 51 keys of the Russian and Latin alphabets, numbers and special characters for recording information in the control device with subsequent display of it on the ELT screen;

a typewriter that permits one to type information coming from the computer or from the display screen.

Unlike the AP-61 and AP-62, the AP-62 (YeS-8563) and AP-64 (YeS-8564) user stations include 24 and 16 ELT displays, respectively, measuring 25 cm in the diagonal

and with working field of 240 characters. Centralized control of the displays and of their corresponding alphanumeric keyboards is accomplished by a group control device having memory with capacity of 4,096 bytes and located at a distance up to 500 meters from the displays. Two typewriters can also be connected to this device. The configuration of the remote processing system utilizing the AP-64 is presented in Figure 13.3.

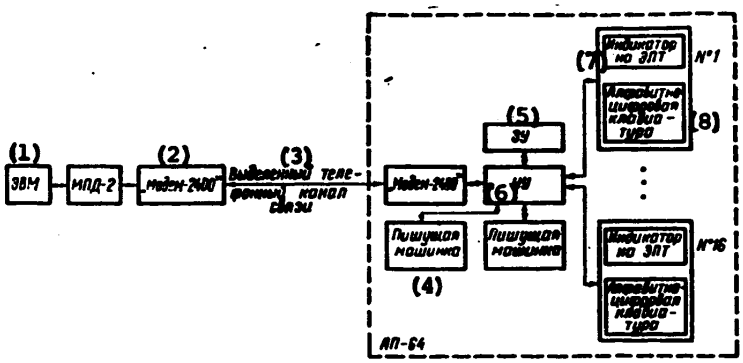

Figure 13.3. Configuration of Remote Data Processing System of Unified Computer System Using AP-64

Key:

1. Computer
2. Modem-2400
3. Segregated telephone communications channel
4. Typewriter
5. Storage device
6. Control unit
7. ELT display
8. Alphanumeric keyboard

The AP-70 user station (YeS-8570) is designed for semiduplex exchange of information over commutated and segregated telephone and uncommutated telegraph communications channels with a computer or other user stations in remote processing systems of the unified computer system. The transmission speed is 100 bauds. The AP-70 is the simplext to operate. It includes a Konsul-260.1 typewriter, modem-200 or signal conversion device. The AP-70 can also be connected to the computer through any data transmission multiplexer. The configuration of the data transmission system using the AP-70 is shown in Figure 13.4.

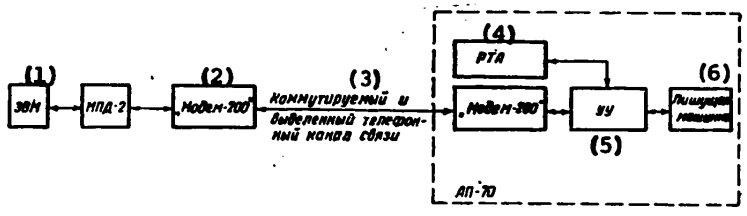

Figure 13.4. Configuration of Remote Data Transmission System of Unified Computer System Using AP-70

[Key on following page]

[Key continued from preceding page]

1. Computer
2. Modem-200
3. Commutated and segregated telephone communications channel
4. Telegraph apparatus
5. Control unit
6. Typewriter

Selection of one or another user station depends on the designation of the remote processing system. Thus, for example, the AP-1, AP-4 and AP-11 can be used for data gathering. The AP-61 to AP-64 user stations, which include displays, are effective in those cases when rapid output of data is required and information must be processed in the computer interaction mode. The AP-11, AP-14, AP-50 and AP-70 may be used in remote data processing when the results are fed to the user station. Moreover, the AP-70 can be used in text editing (for retrieval and output of documents, modification of them and return to the system for subsequent processing). The AP-5 and AP-6 are most effective to monitor and control production.

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